Session 9:   Solid State Physics

MOS Cap

Outline

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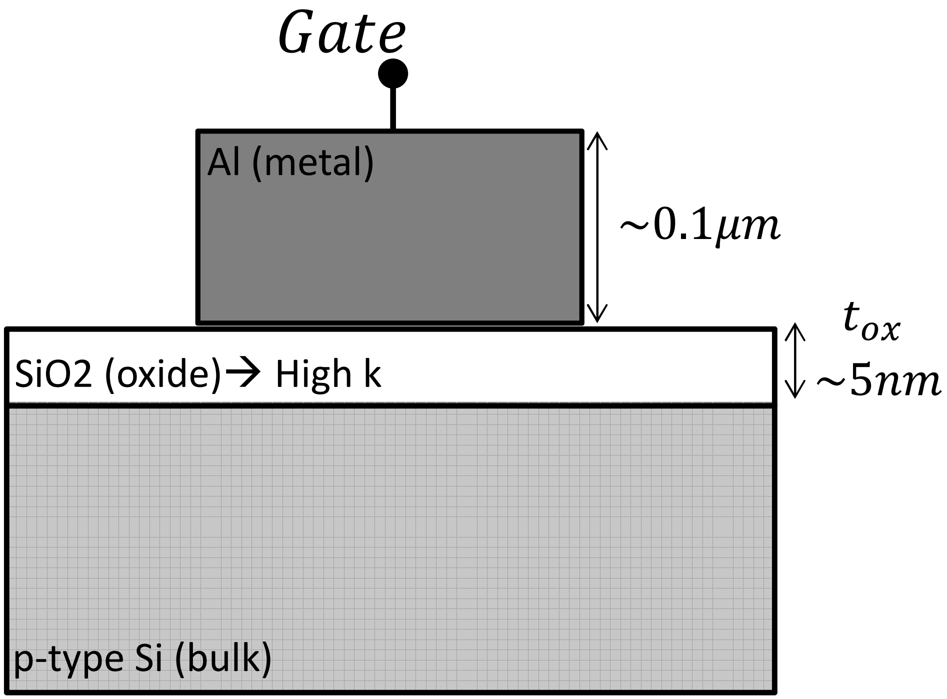
- A
  - B
  - C
  - D
  - E
- F
  - G
- H
- I
- J

MOS!

Metal:	Al, …, Poly Si (n++,p++), $\rho_{poly} = 0.1\ m\Omega cm$
Oxide:	SiO2 (reason why Si beat GaAs)
Semi Conductor:	Si

CMOS is the dominant technology in integrated circuits

Heart of a MOSFET is MOS-cap



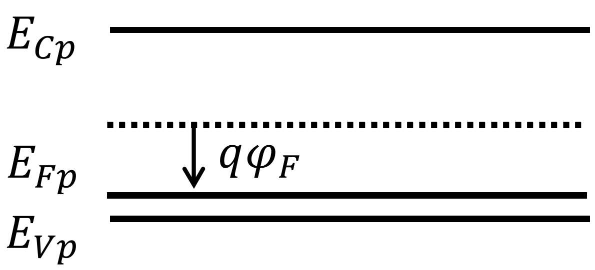
p-type bulk → nMOS
n-type bulk → pMOS
(n/p)MOS → CMOS

$\epsilon_{Si} = 11.9$, $(\sim 3\times)\epsilon_{SiO_2} = 3.9$

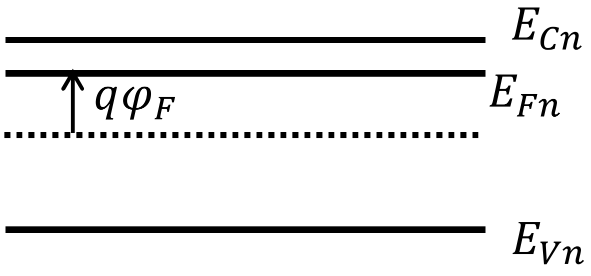
Bulk Semiconductor Potential , φ_F

Definition:

$$q\varphi_F \equiv E_i - E_F = E_{i(bulk)} - E_F$$



p-type



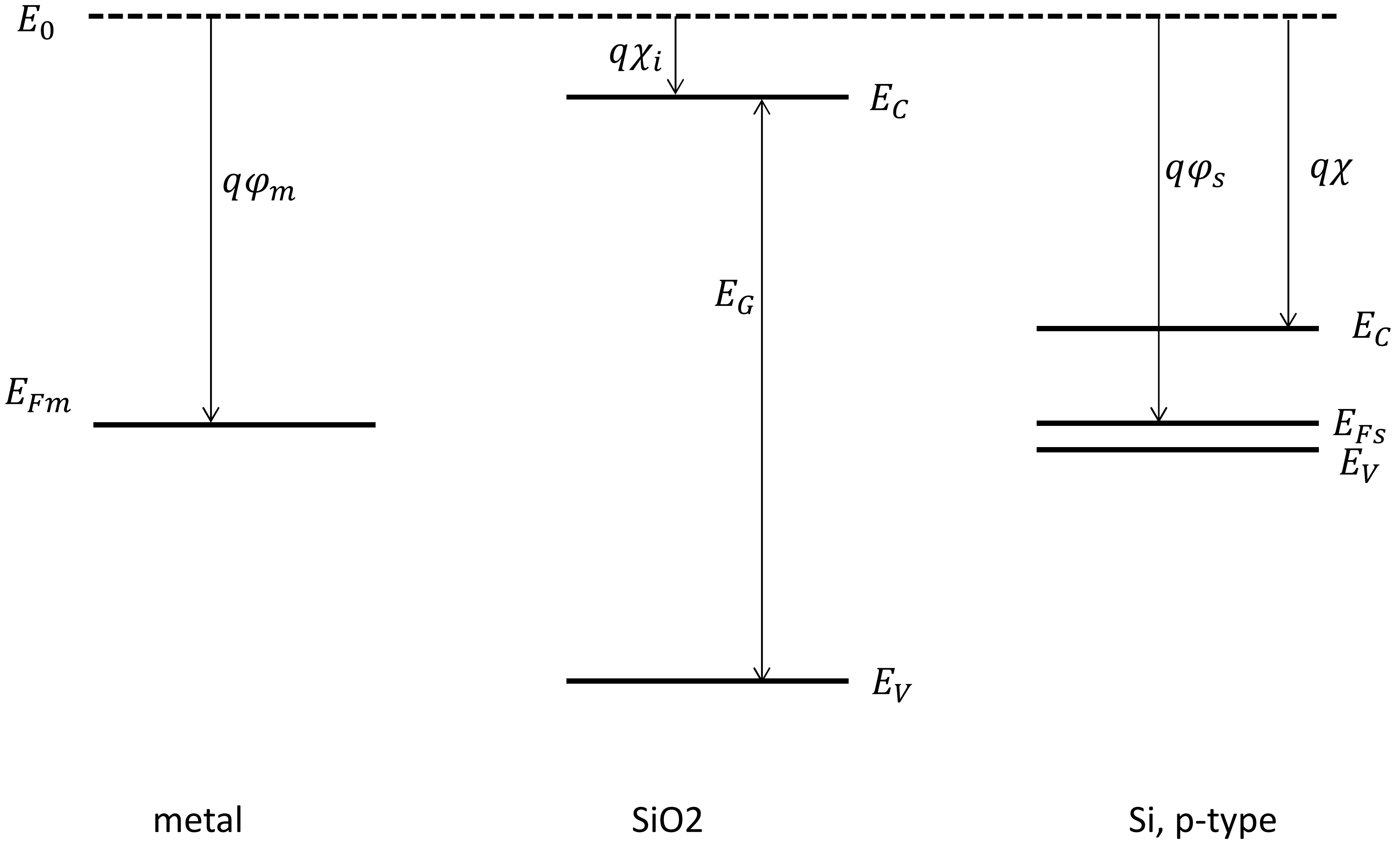
n-type

$$\varphi_F = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) > 0$$

$$\varphi_F = -\frac{kT}{q}\ln\left(\frac{N_D}{n_i}\right) < 0$$

MOS – Special Case

Special case: $\varphi_m = \varphi_s$



MOS – Special Case

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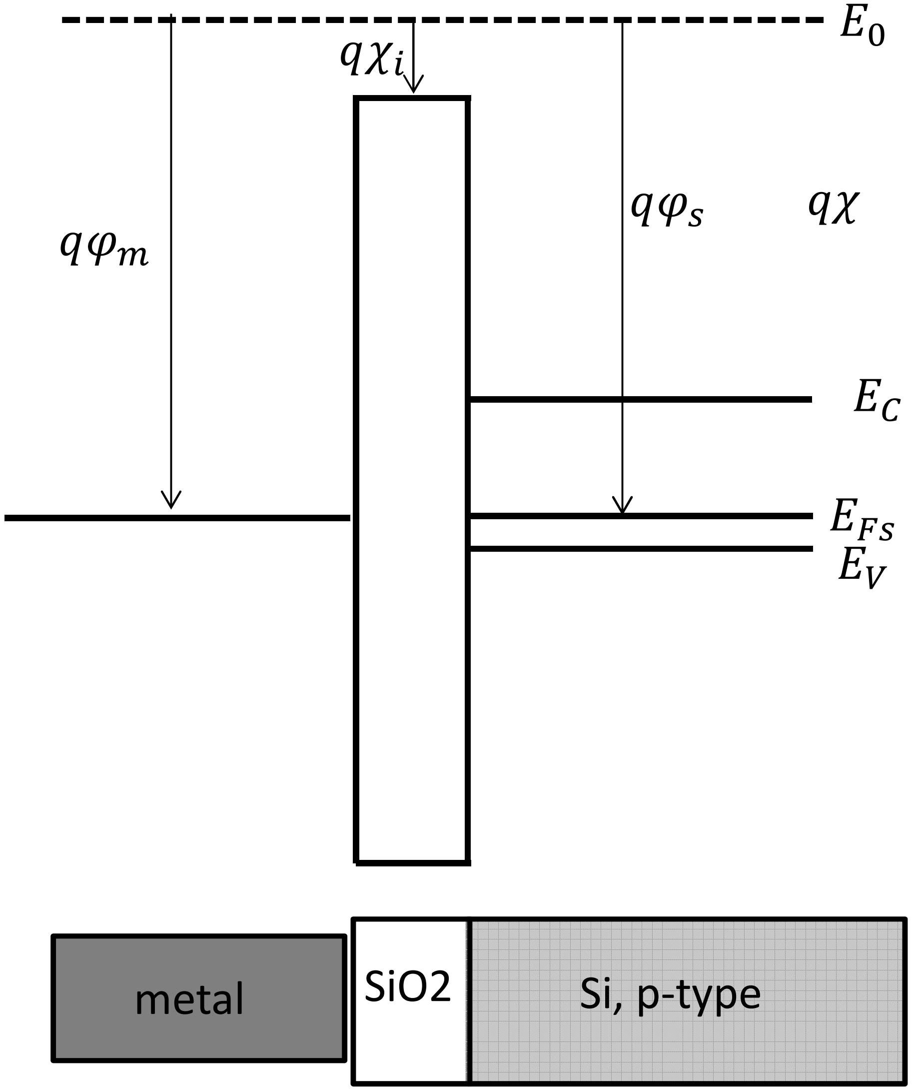
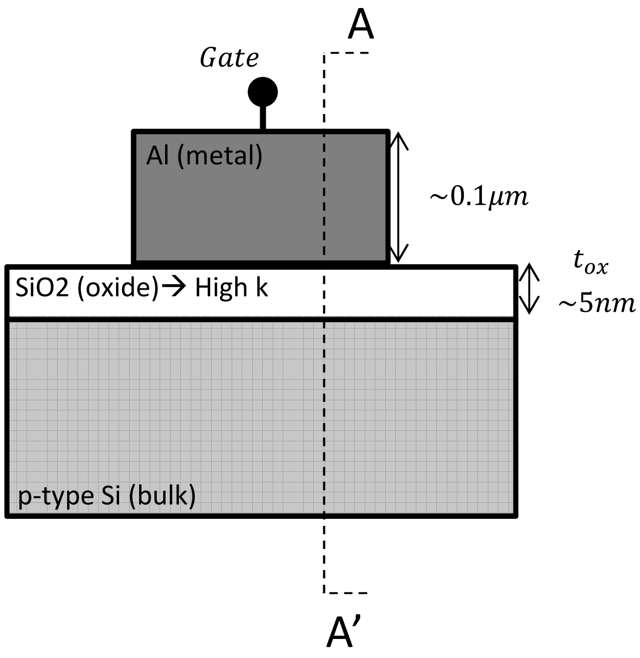
Special case: $\varphi_m = \varphi_s$





M (Al) , O (SiO2) , S (Si)

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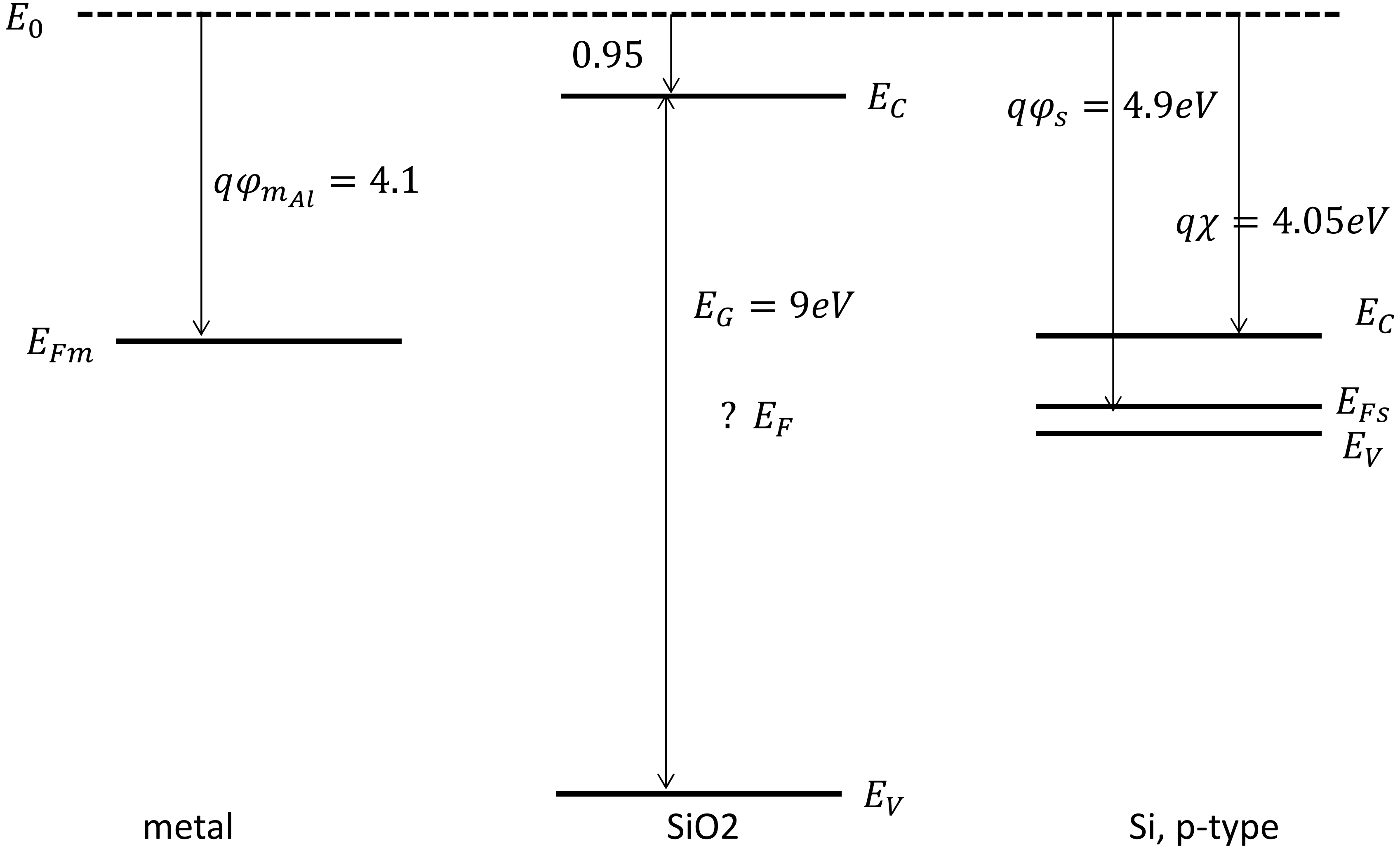
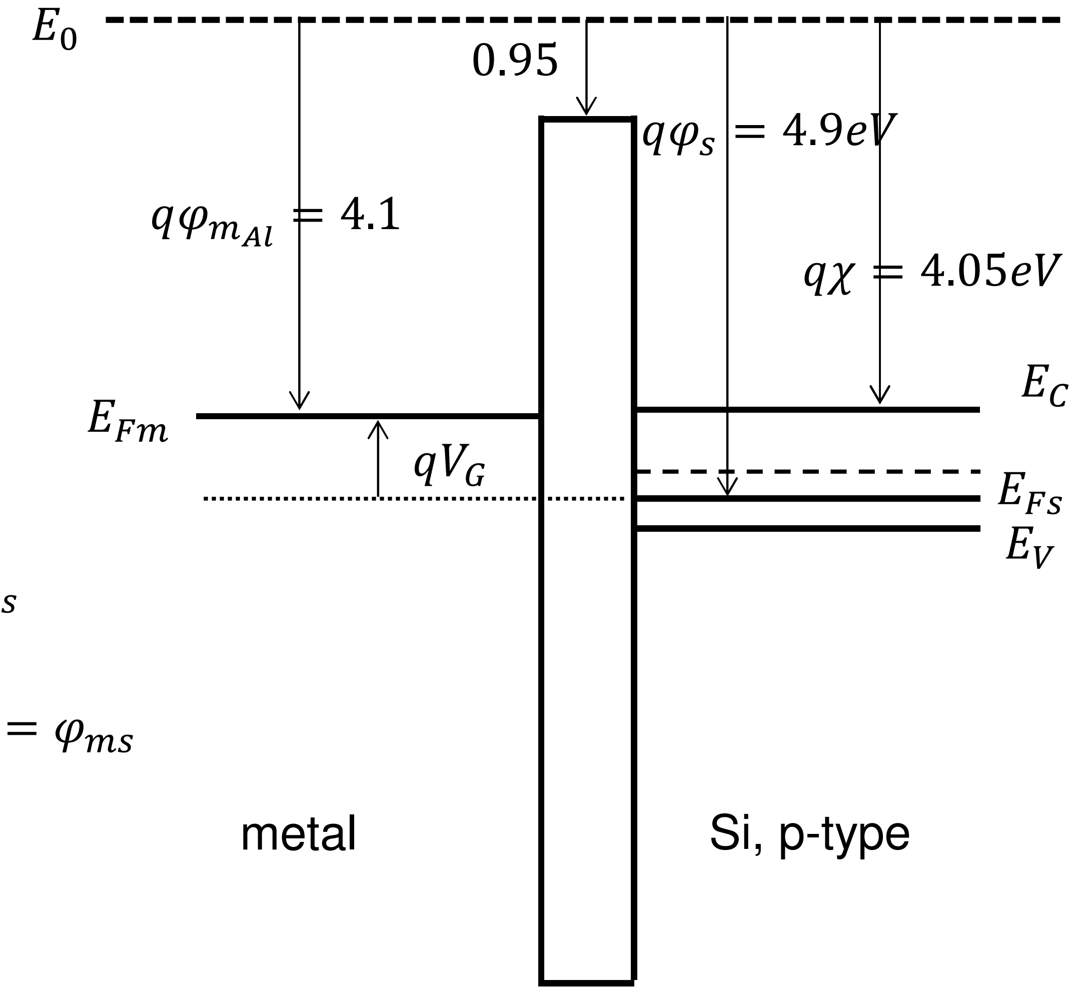


Flat Band Voltage

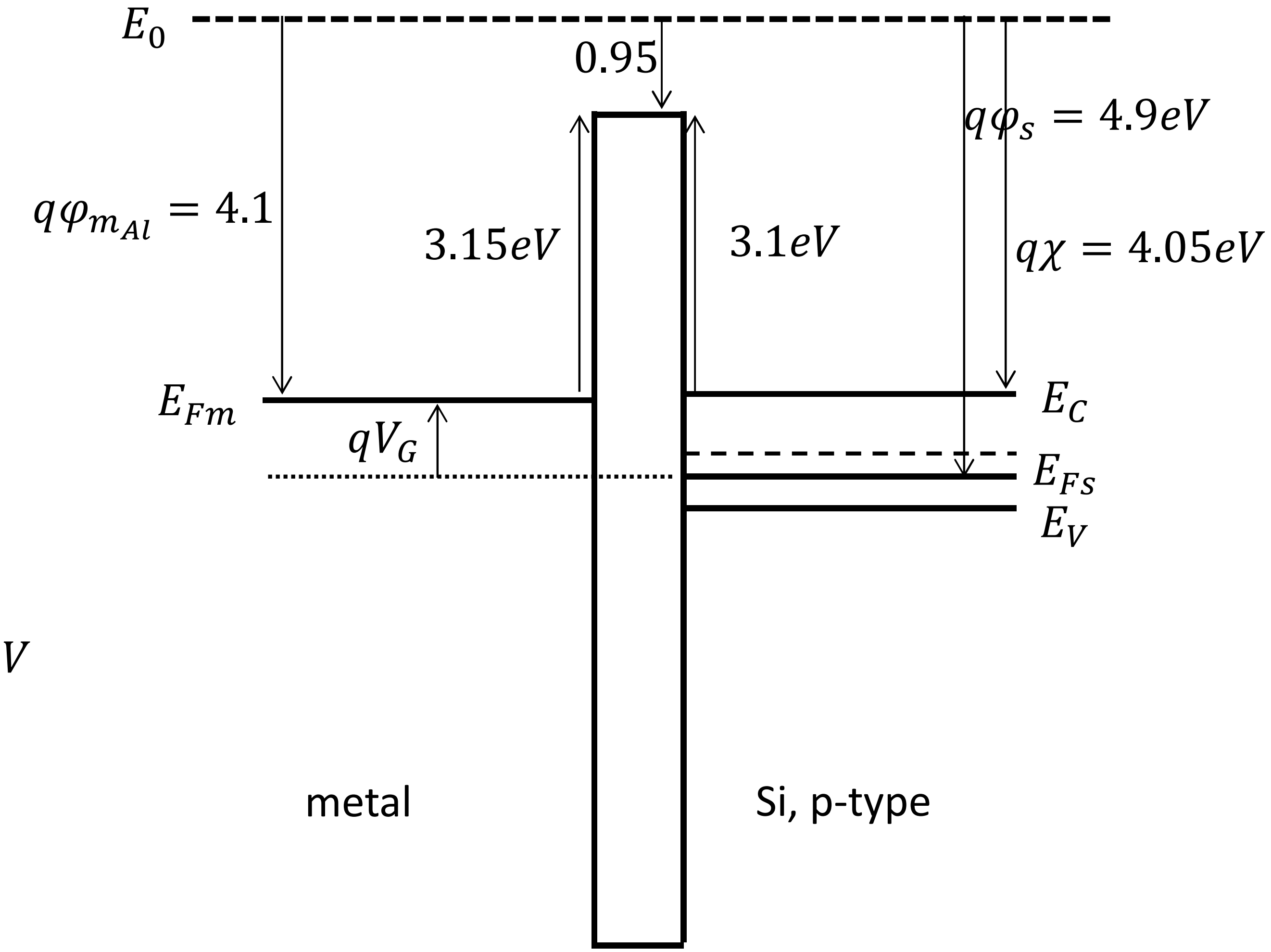


$$qV_G = q\varphi_m - q\varphi_s$$

$$V_{FB} \equiv \varphi_m - \varphi_s = \varphi_{ms}$$

$$V_{FB} = -0.8\,V$$

Voltage Barrier



$V_G = V_{FB} = -0.8\ V$

No way electrons might pass the voltage barrier!

No Gate Voltage

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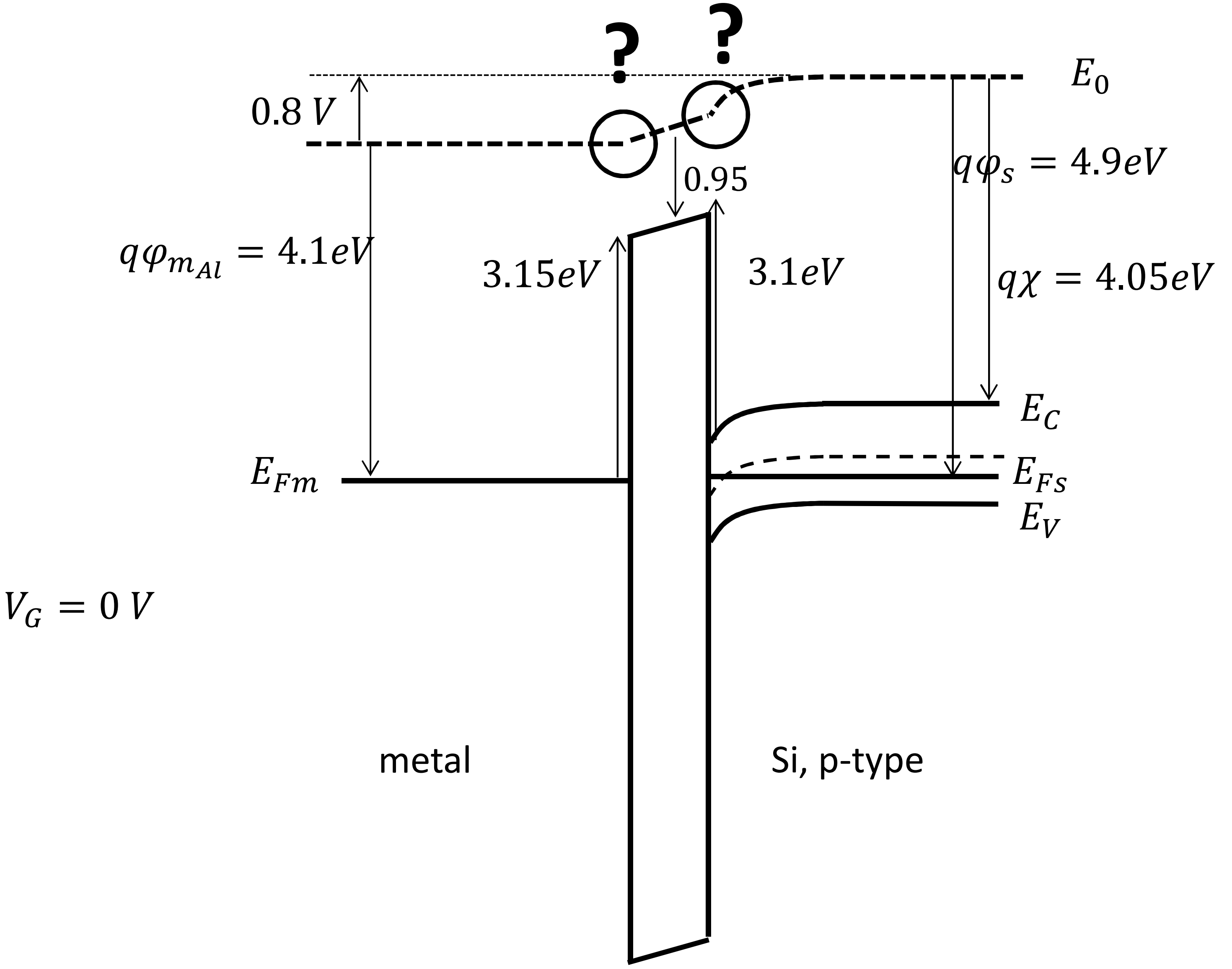
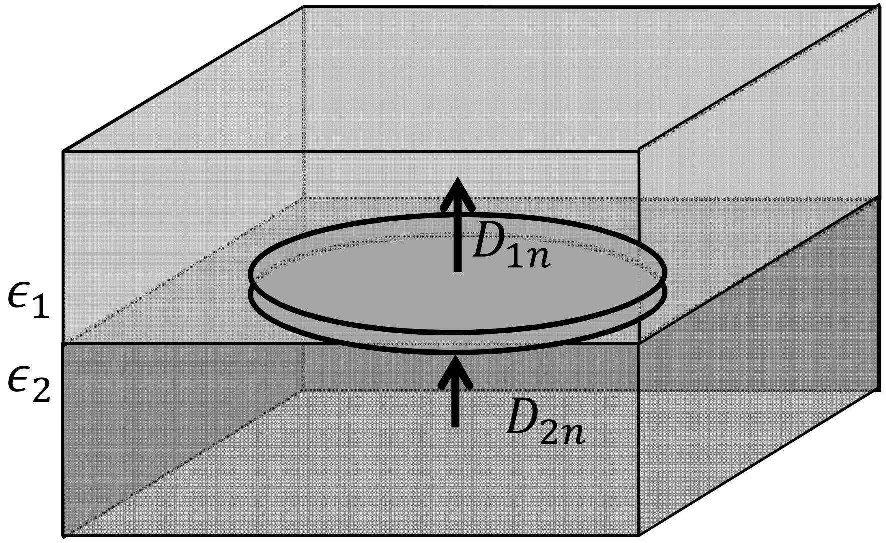


Boundary Condition



$$D_{2n} - D_{1n} = \rho_{surfacce}$$

$$\rho_{surfacce} = 0$$

$$\epsilon_1 \mathcal{E}_1 = \epsilon_2 \mathcal{E}_2$$

$$\epsilon_{Ox} \left.\frac{dE_{Ox}}{dx}\right|_{int} = \epsilon_{Si} \left.\frac{dE_{Si}}{dx}\right|_{int}$$

$$\left.\frac{dE_{Ox}}{dx}\right|_{int} \cong 3 \left.\frac{dE_{Si}}{dx}\right|_{int}$$

M (PolyGate) , O (SiO2) , S (Si)

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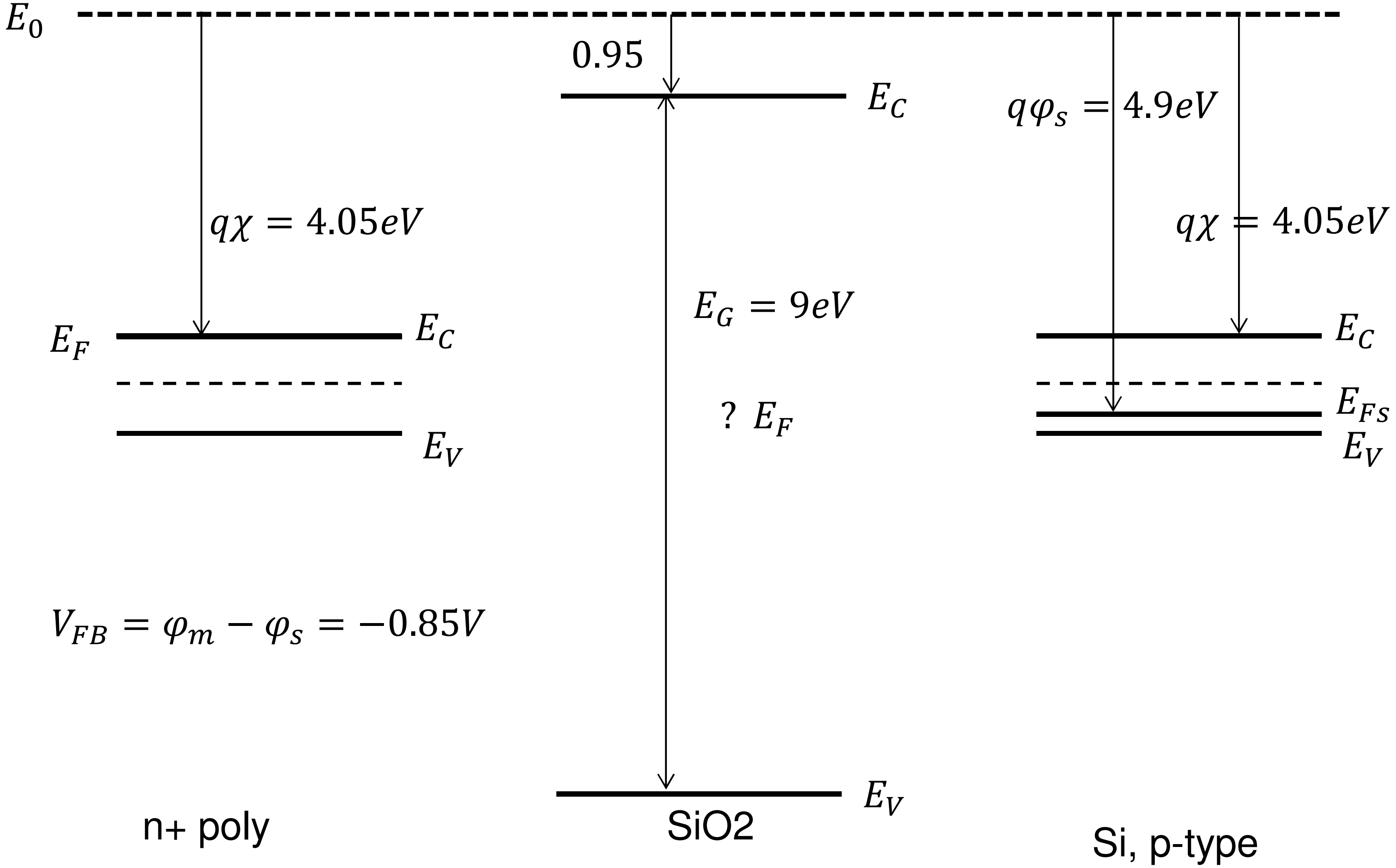


E_0

0.95

E_C

$q\varphi_s = 4.9eV$

$q\chi = 4.05eV$

$E_G = 9eV$

$q\chi = 4.05eV$

E_F

E_C

E_C

$?\ E_F$

E_{Fs}

E_V

E_V

$V_{FB} = \varphi_m - \varphi_s = -0.85V$

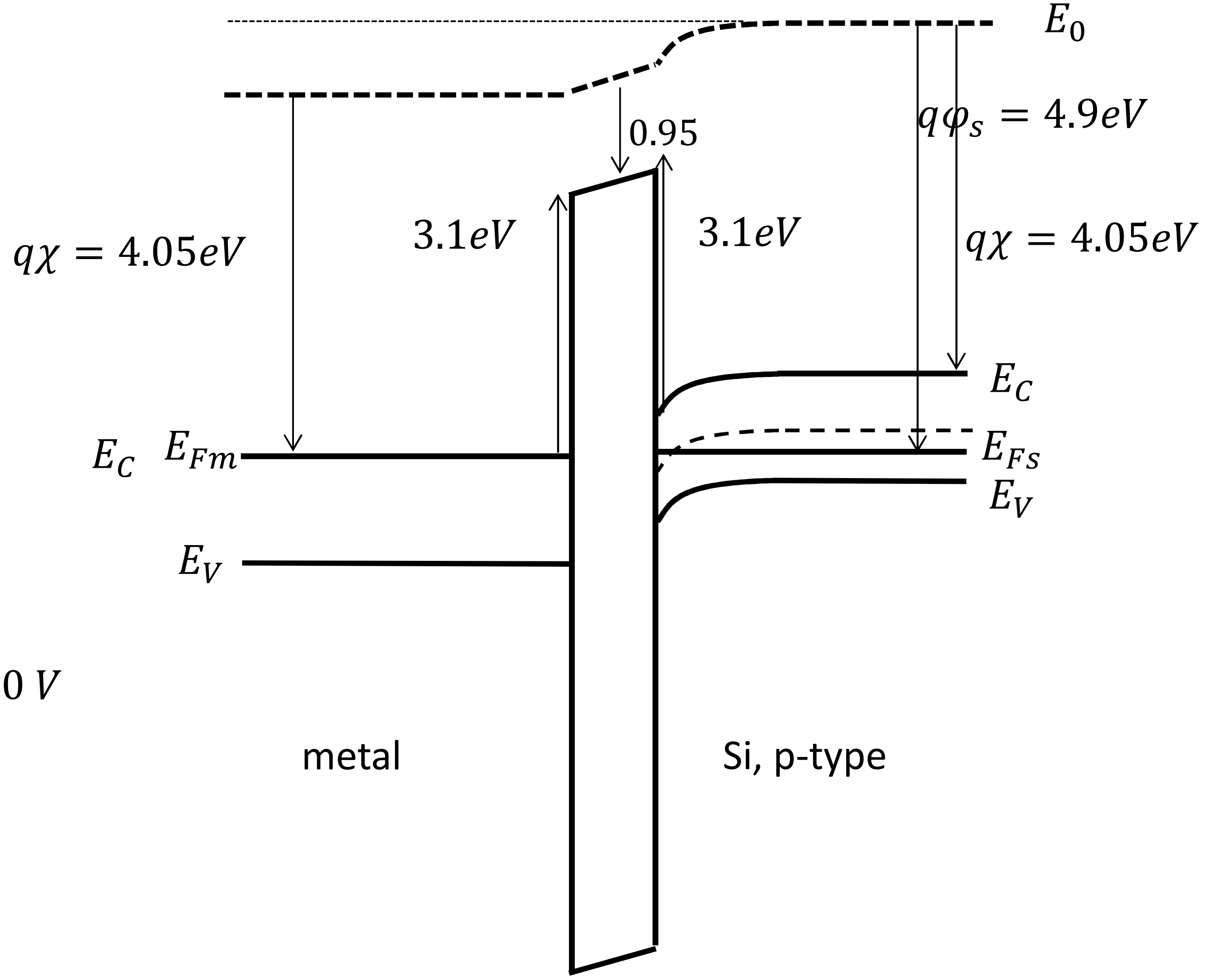
E_V

n+ poly

SiO2

Si, p-type

No Gate Voltage – Poly Gate



$V_G = 0\ V$

No Gate Voltage

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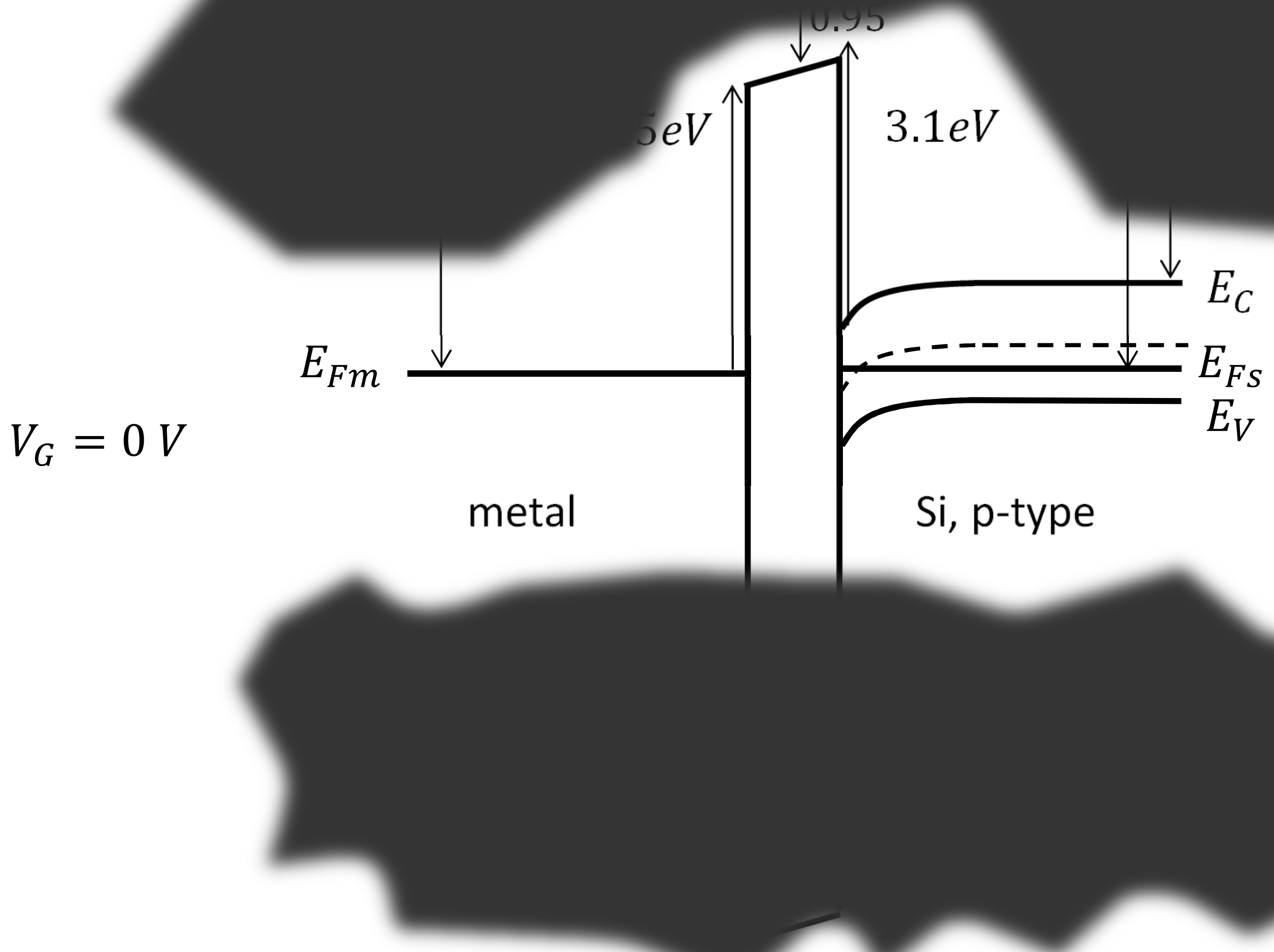

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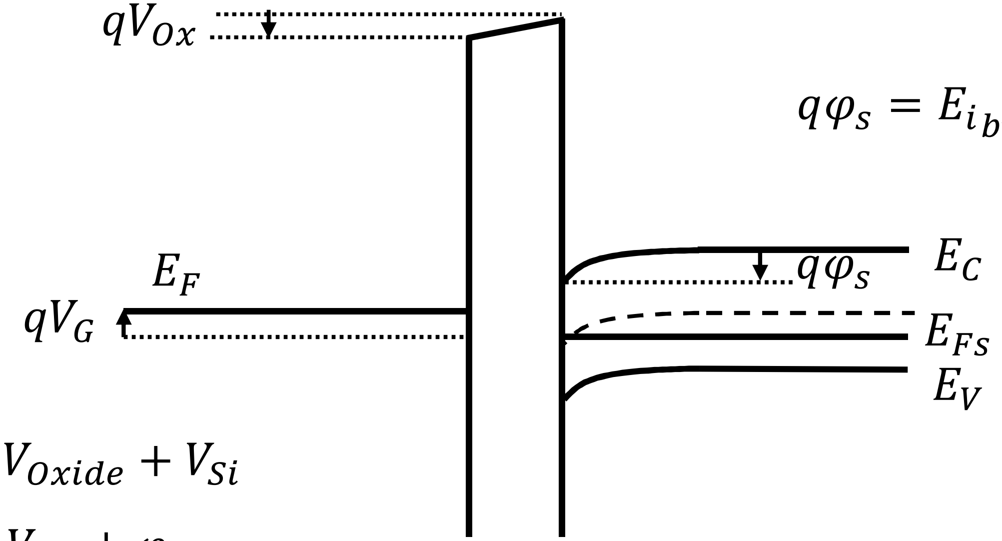
No Gate Voltage



$$q\varphi_s = E_{i_{bulk}} - E_{i_{surface}}$$

$$V_G - V_{FB} = V_{Oxide} + V_{Si}$$
$$= V_{Ox} + \varphi_s$$

$$\boxed{V_G - V_{FB} = V_{Ox} + \varphi_s}$$

As important as KVL

Flat Band

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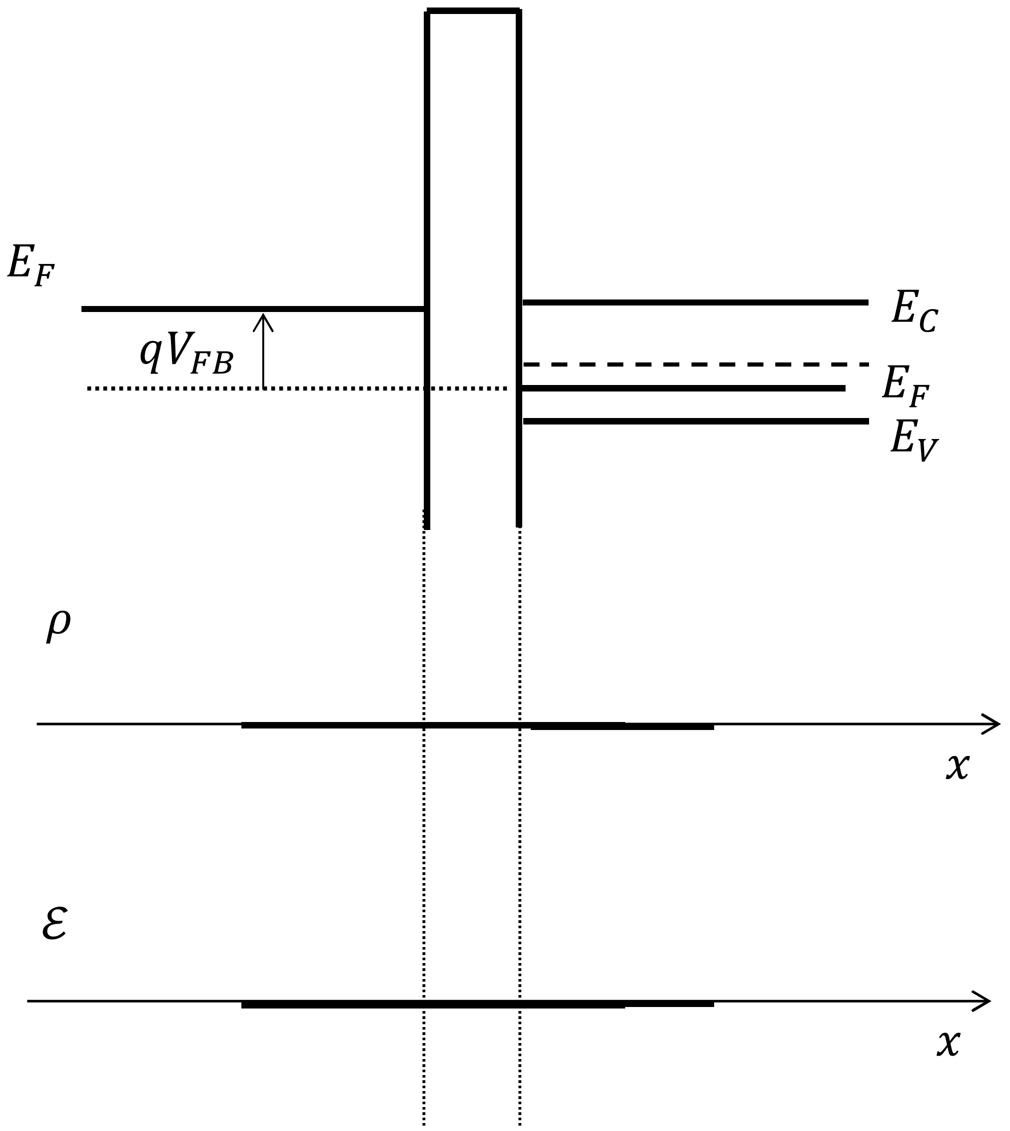
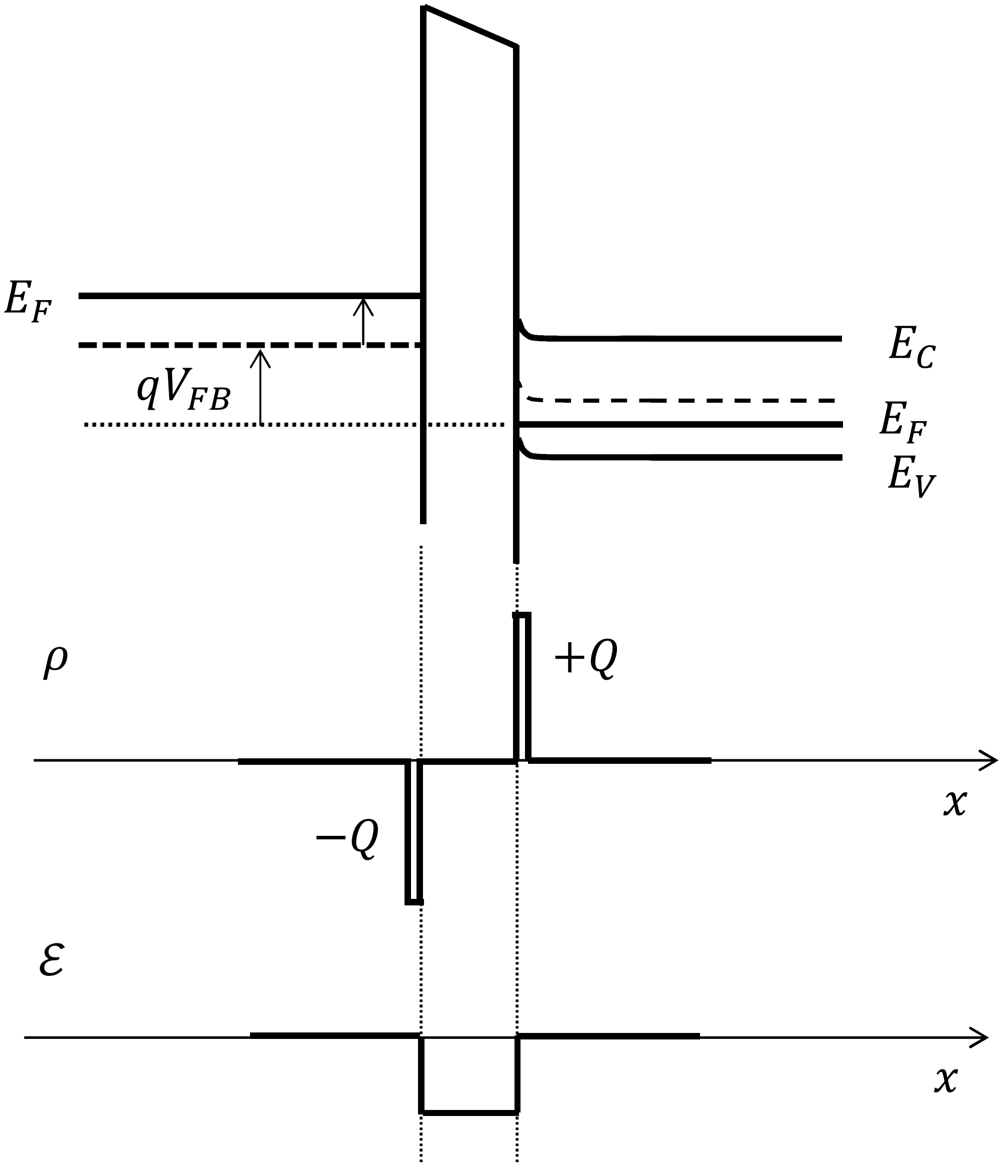
$V_G = V_{FB}$



Accumulation

$V_G < V_{FB}$



Flat Band

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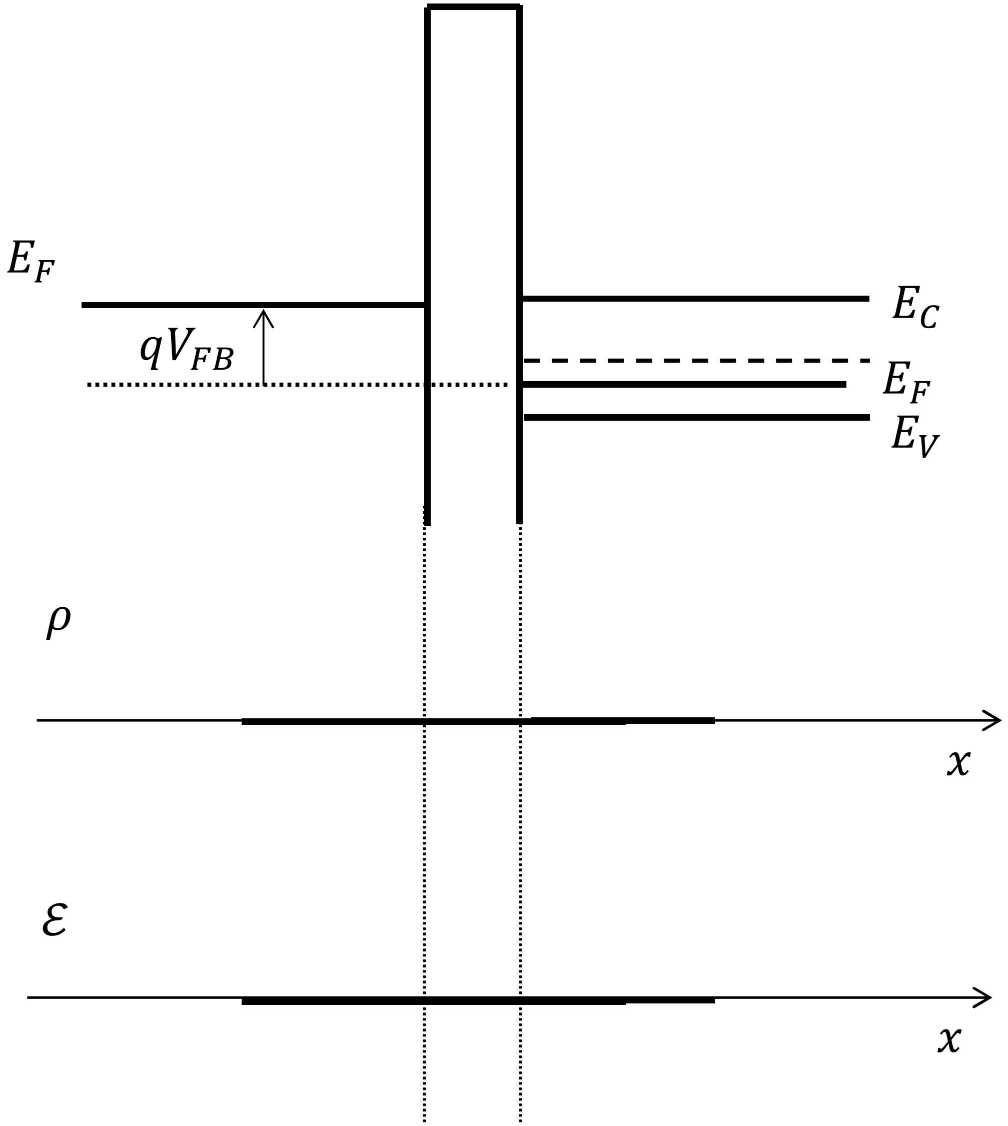
$V_G = V_{FB}$



Depletion (Weak Inversion)

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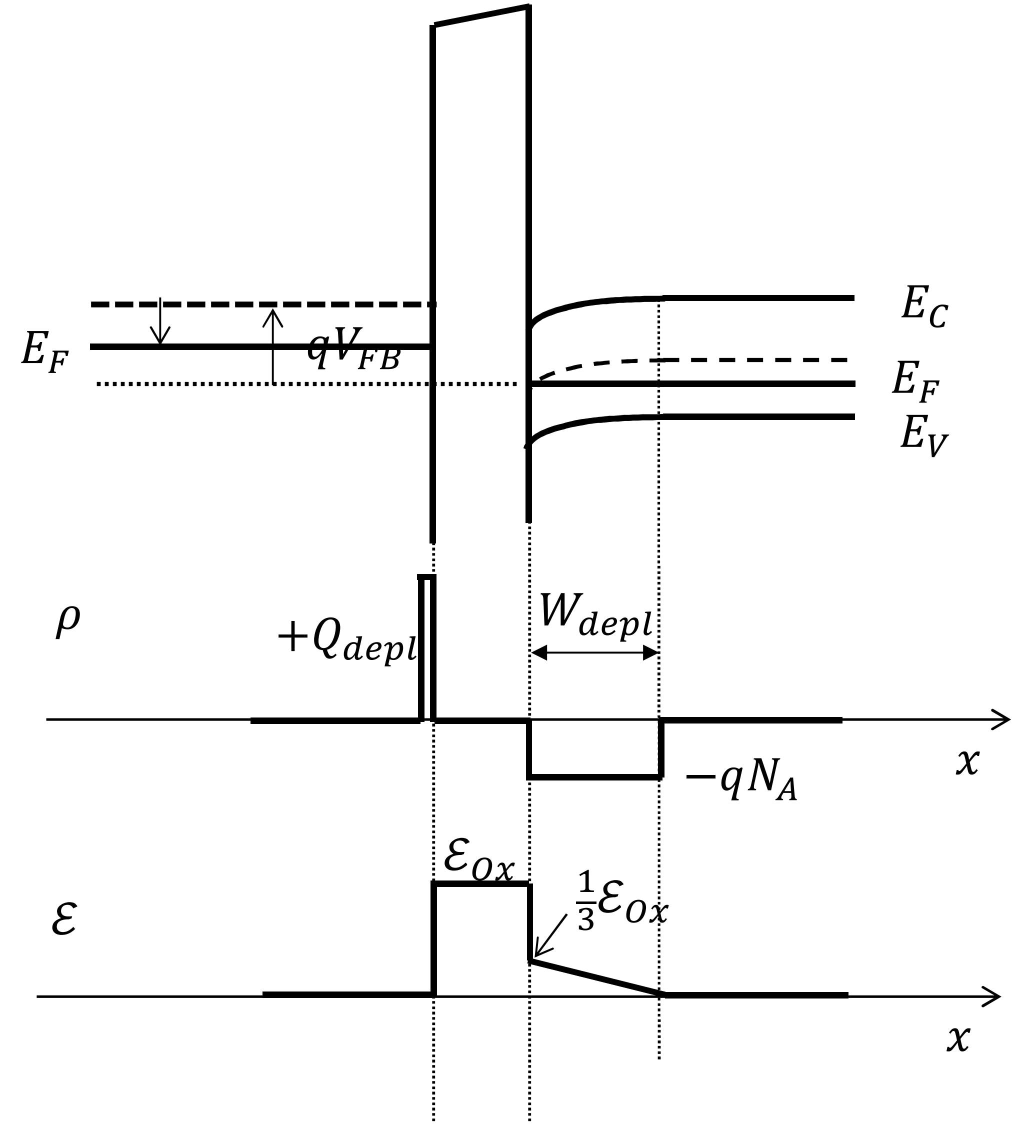
$V_T > V_G > V_{FB}$



(Strong) Inversion

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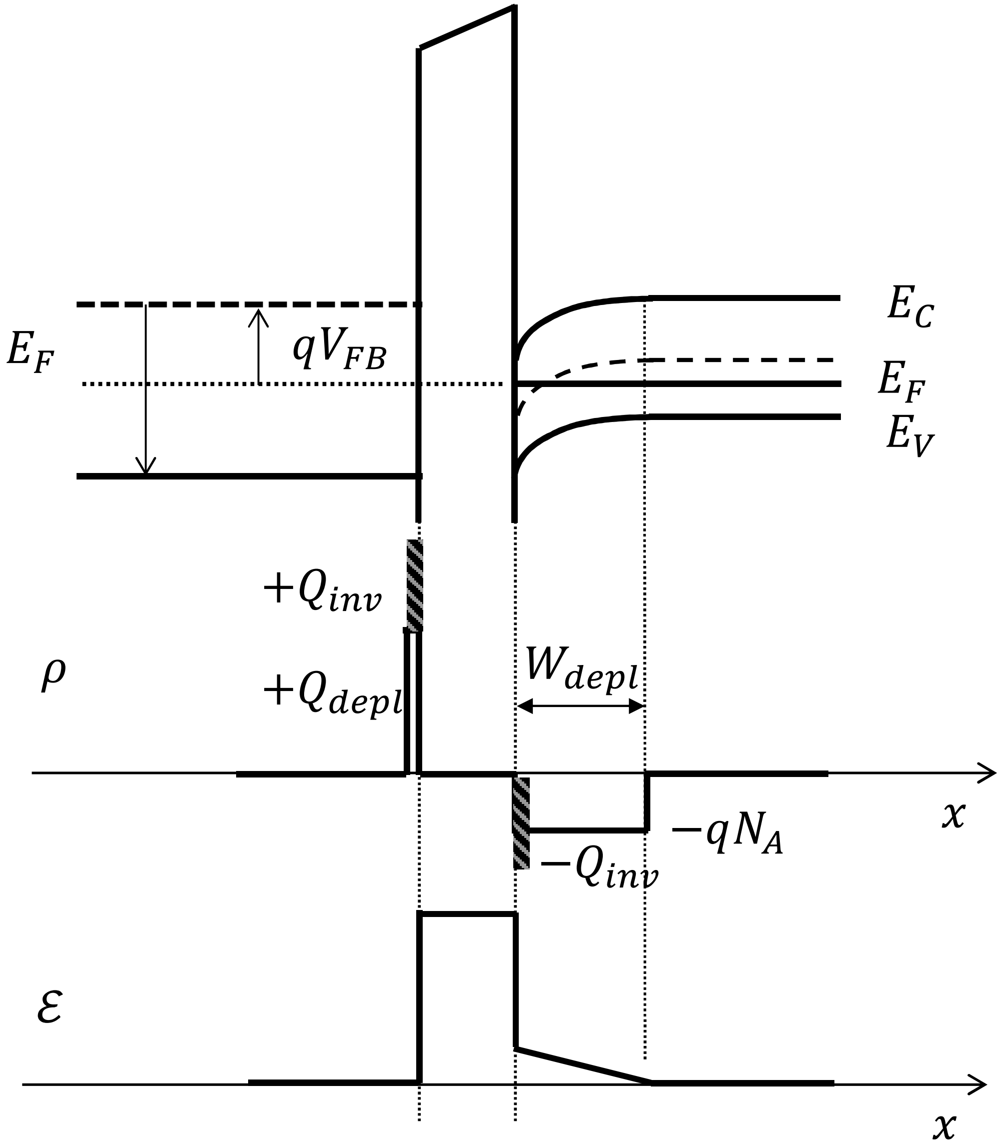
$V_G > V_T$



Depletion (Weak Inversion)

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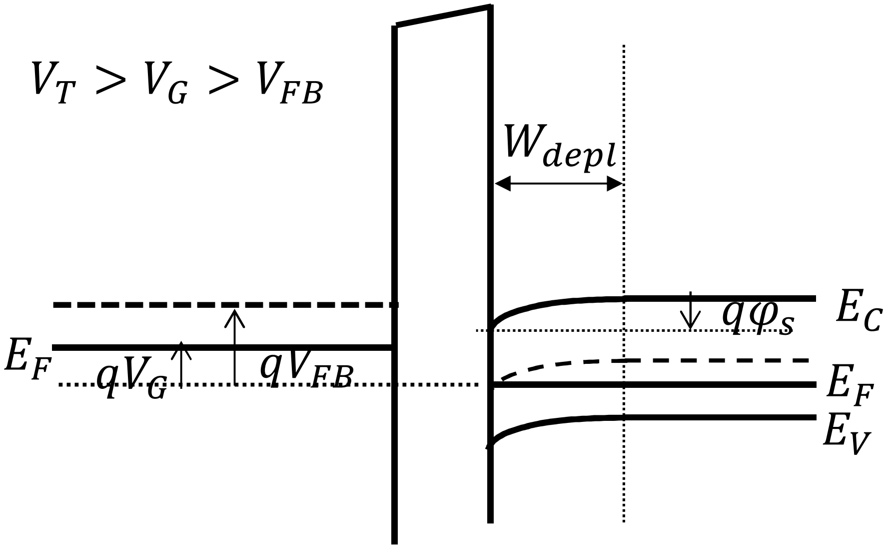
$V_T > V_G > V_{FB}$



$$\frac{d\mathcal{E}}{dx} = \frac{\rho}{\epsilon_{Si}} = \frac{-qN_A}{\epsilon_{Si}} = \frac{d^2\varphi}{dx^2}$$

$$\rightarrow \varphi_s = \frac{qN_A x^2}{2\epsilon_{Si}} \qquad \rightarrow W_d = \sqrt{\frac{2\epsilon_{Si}}{qN_A}\varphi_s}$$

$$Q_{dep} = -qN_A W_d = \sqrt{2qN_A\epsilon_{Si}\varphi_s}$$

$$\mathcal{E}_{Ox} = \frac{-Q_{dep}}{\epsilon_{Ox}} \qquad \rightarrow V_{Ox} = \frac{-t_{ox}Q_{dep}}{\epsilon_{Ox}} = \frac{-Q_{dep}}{C_{Ox}} \quad \begin{matrix}[C/cm^2] \\ [F/cm^2]\end{matrix}$$

$$V_G = V_{FB} + V_{Ox} + \varphi_s \rightarrow \boxed{V_G = V_{FB} + \varphi_s + \frac{1}{C_{Ox}}\sqrt{2qN_A\epsilon_{Si}\varphi_s}}$$

p-type Si (nMOS)
In Depl

$$\varphi_s < 0 \qquad \boxed{V_G = V_{FB} + \varphi_s - \frac{1}{C_{Ox}}\sqrt{2qN_A\epsilon_{Si}|\varphi_s|}}$$

n-type Si (pMOS)
In Depl

Threshold Voltage – Definition!

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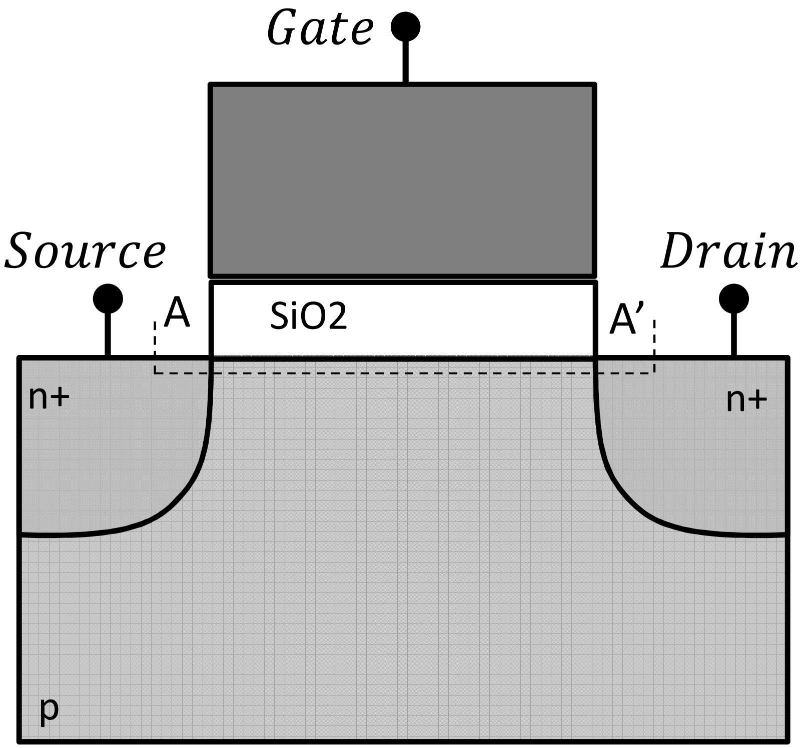
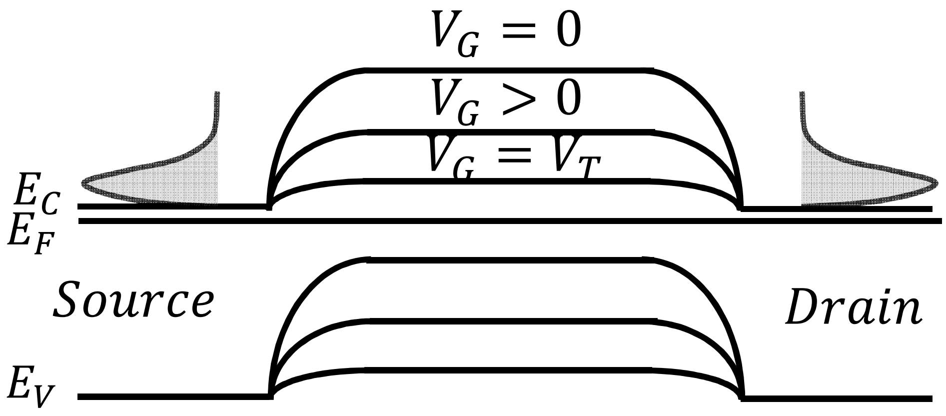
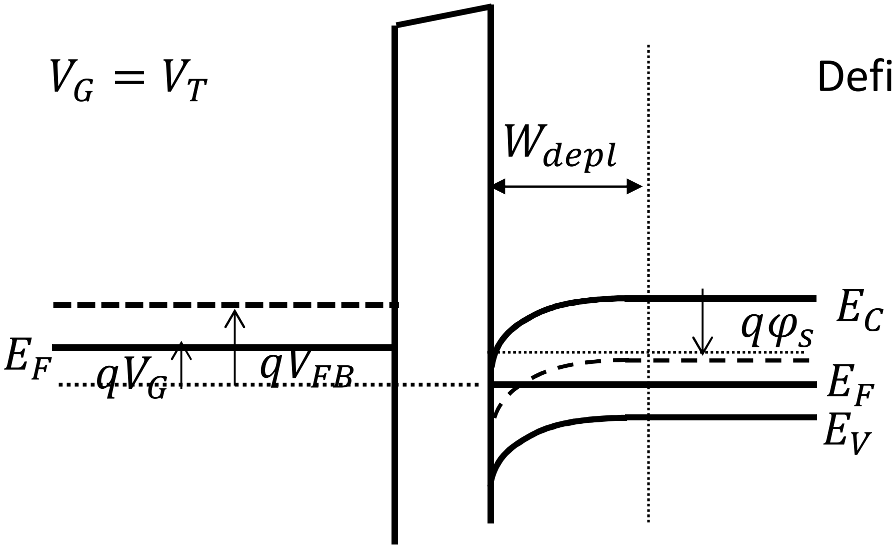




Threshold Voltage

$V_G = V_T$



Definition of Threshold voltage:

$$V_T = V_G\Big|_{\varphi_s = 2\varphi_F}$$

$$p_{bulk} = N_A \qquad n_{surface} = N_A$$

$$W_{max} = W_{depl}\Big|_{\varphi_s = 2\varphi_F} = \sqrt{\frac{2\epsilon_{Si}}{qN_A}(2\varphi_F)}$$

p-type

$$V_T = V_G\Big|_{\varphi_s = 2\varphi_F} = V_{FB} + 2\varphi_F + \frac{1}{C_{Ox}}\sqrt{2qN_A\epsilon_{Si}(2\varphi_F)}$$

$$q\varphi_F = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) > 0$$

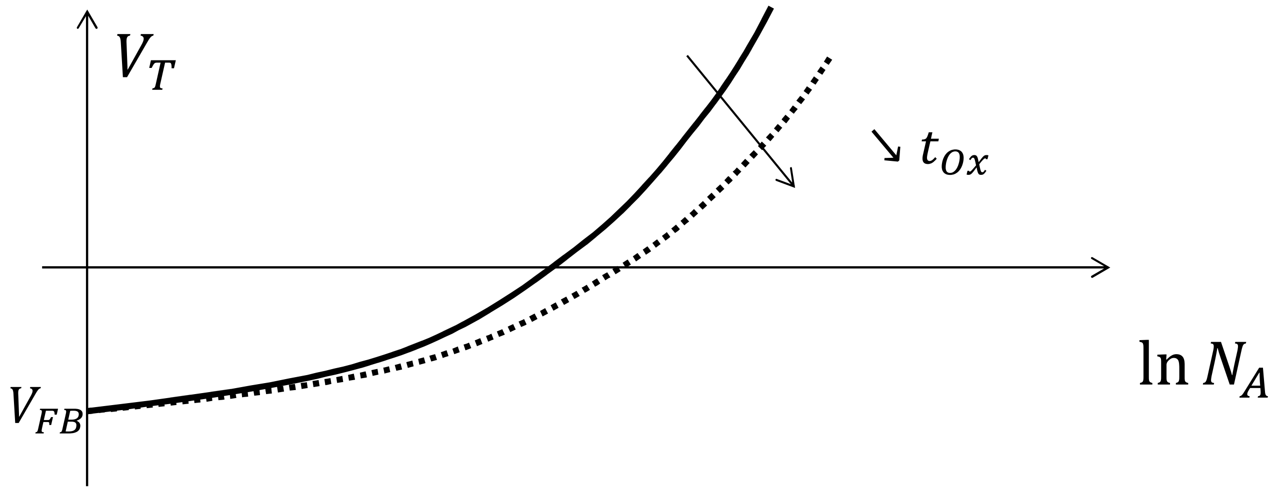
n-type

$$V_G = V_{FB} + 2\varphi_F - \frac{1}{C_{Ox}}\sqrt{2qN_A\epsilon_{Si}|2\varphi_F|}$$

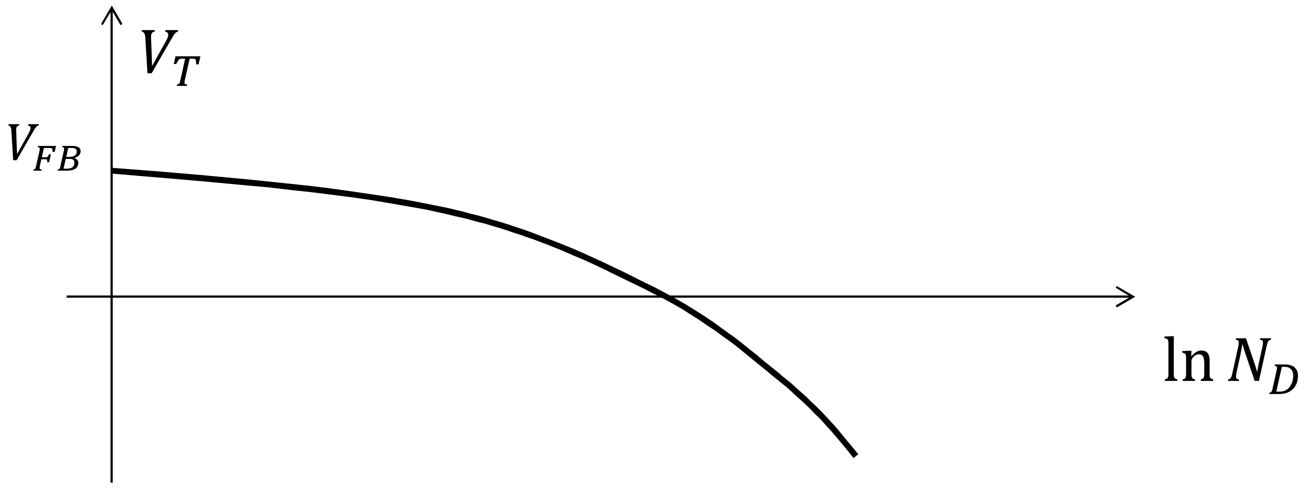
$$q\varphi_F = -\frac{kT}{q}\ln\left(\frac{N_D}{n_i}\right) < 0$$

Threshold Voltage vs. Bulk Doping

p-type

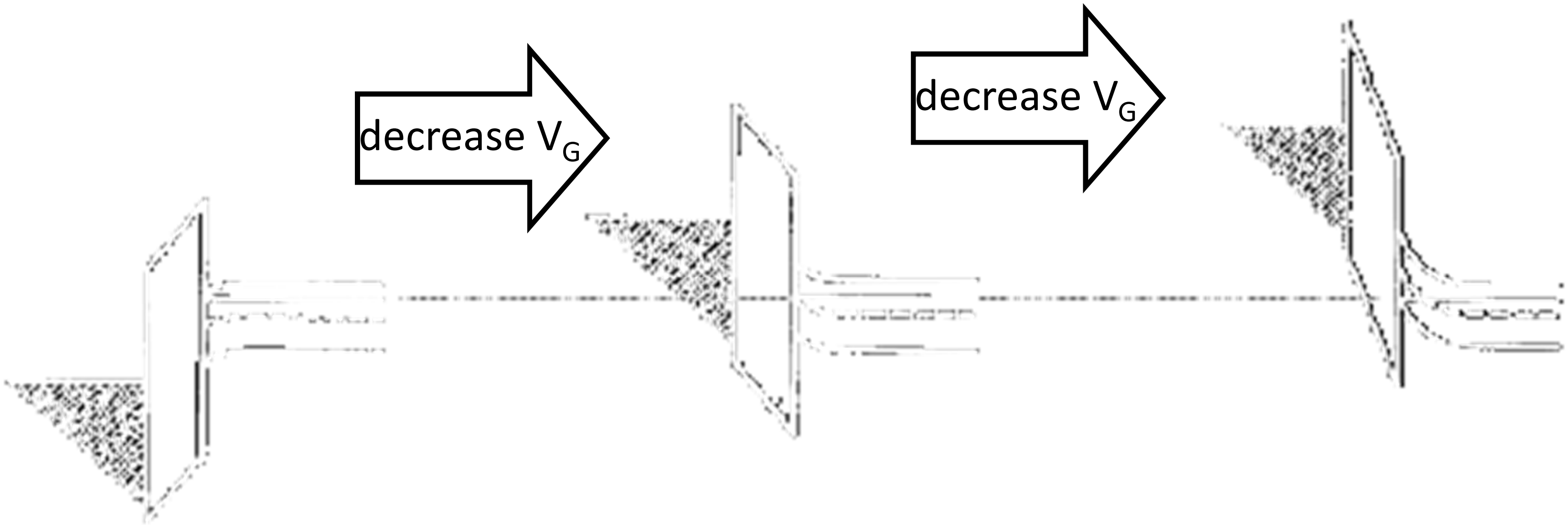


n-type



MOS Band Diagram (n-type Bulk)

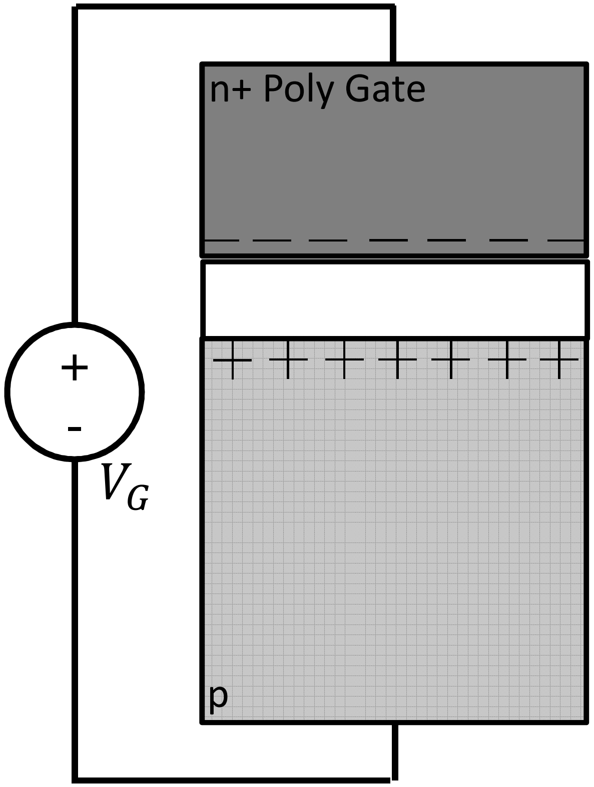
Decrease VG (toward more negative values)
→ move the gate energy-bands up, relative to the Si

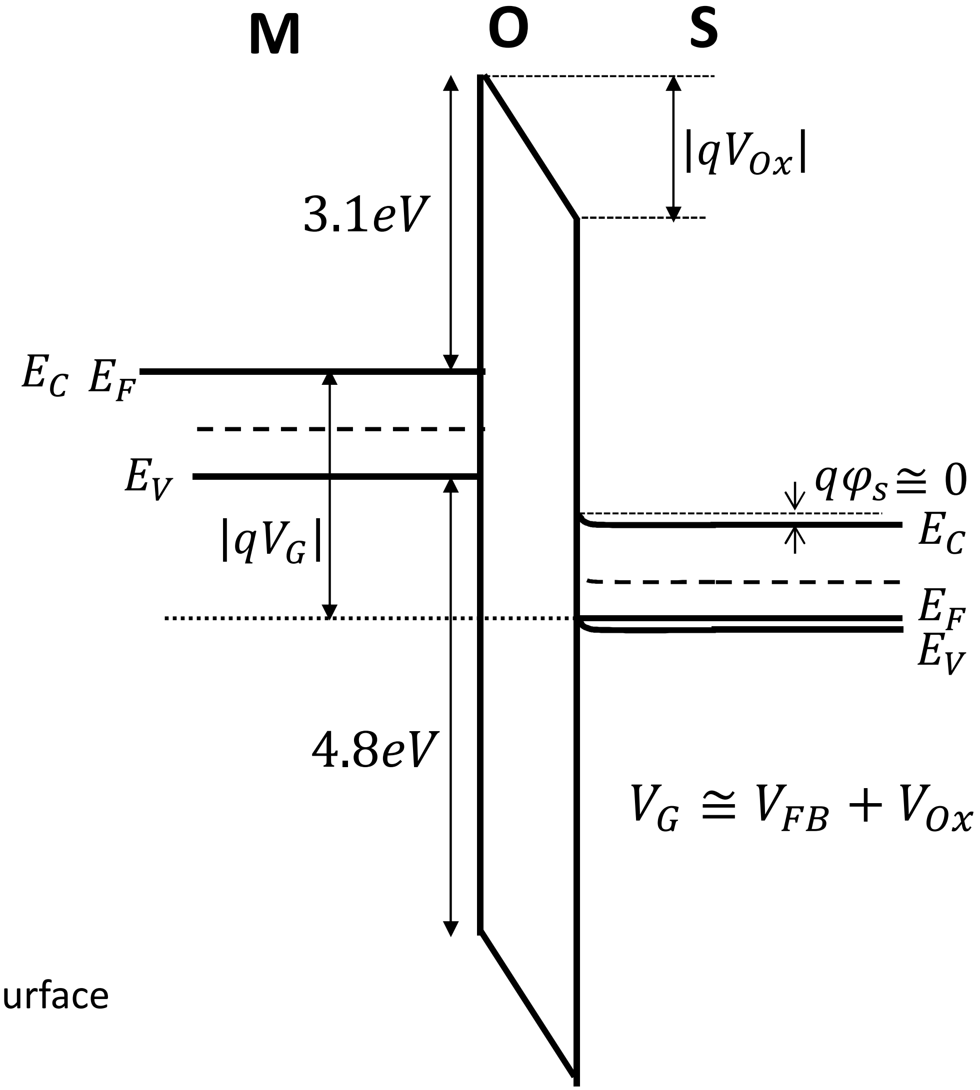


- Accumulation
  - $V_G > V_{FB}$
  - Electrons accumulate at surface
- Depletion
  - $V_G < V_{FB}$
  - Electrons repelled from surface
- Inversion
  - $V_G < V_T$
  - Surface becomes p-type

Accumulation, Poly Gate

$V_G < V_{FB}$





$V_G \cong V_{FB} + V_{Ox}$

Mobile carriers (holes) accumulate at Si surface

Accumulation, Layer Charge Density

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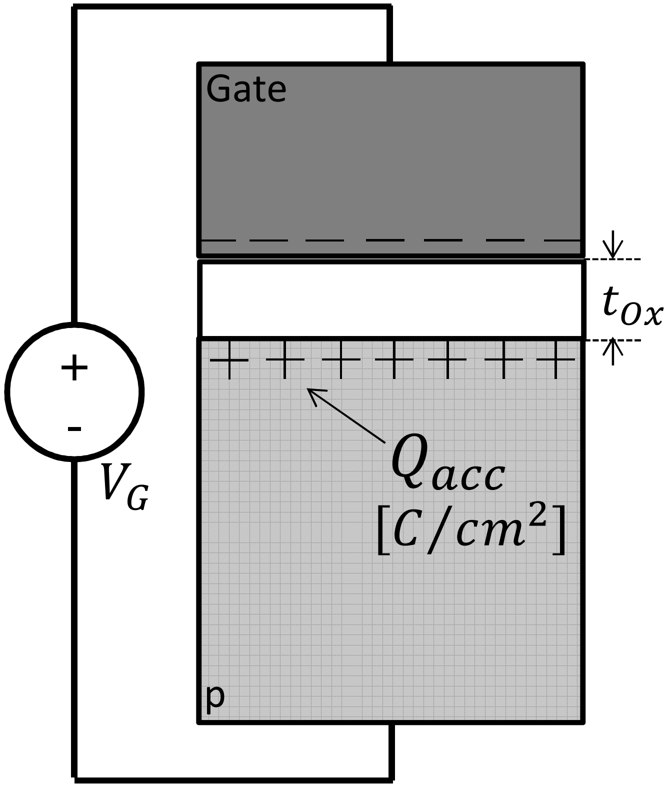
$V_G < V_{FB}$



$$V_{Ox} \cong V_G - V_{FB}$$

From Gauss' Law:

$$\mathcal{E}_{Ox} = -Q_{acc}/\epsilon_{SiO_2}$$

$$V_{Ox} = t_{Ox}\mathcal{E}_{Ox} = -Q_{acc}/C_{Ox}$$

where $C_{Ox} \equiv \epsilon_{SiO_2}/t_{Ox} \qquad [F/cm^2]$

$$\rightarrow \boxed{Q_{acc} = -C_{Ox}(V_G - V_{FB}) > 0}$$

Depletion, Poly Gate

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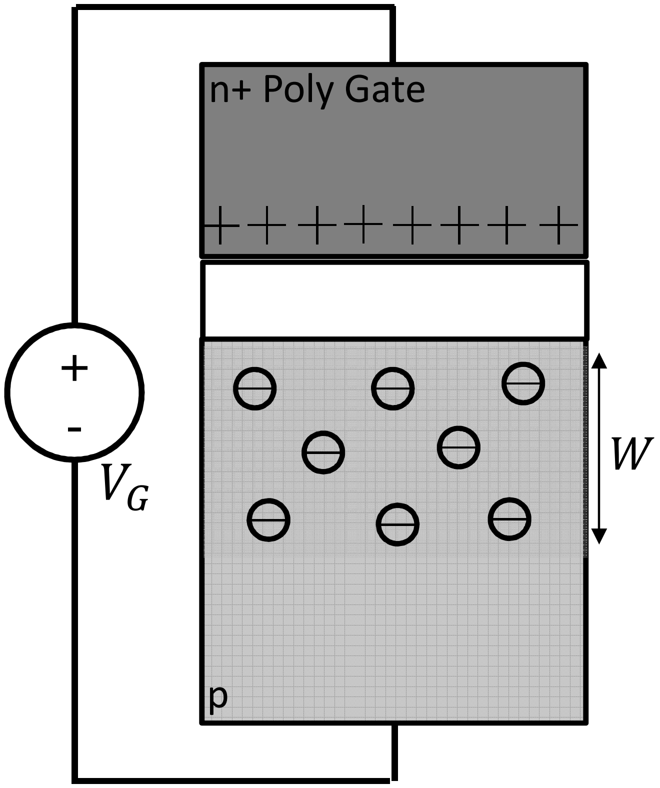
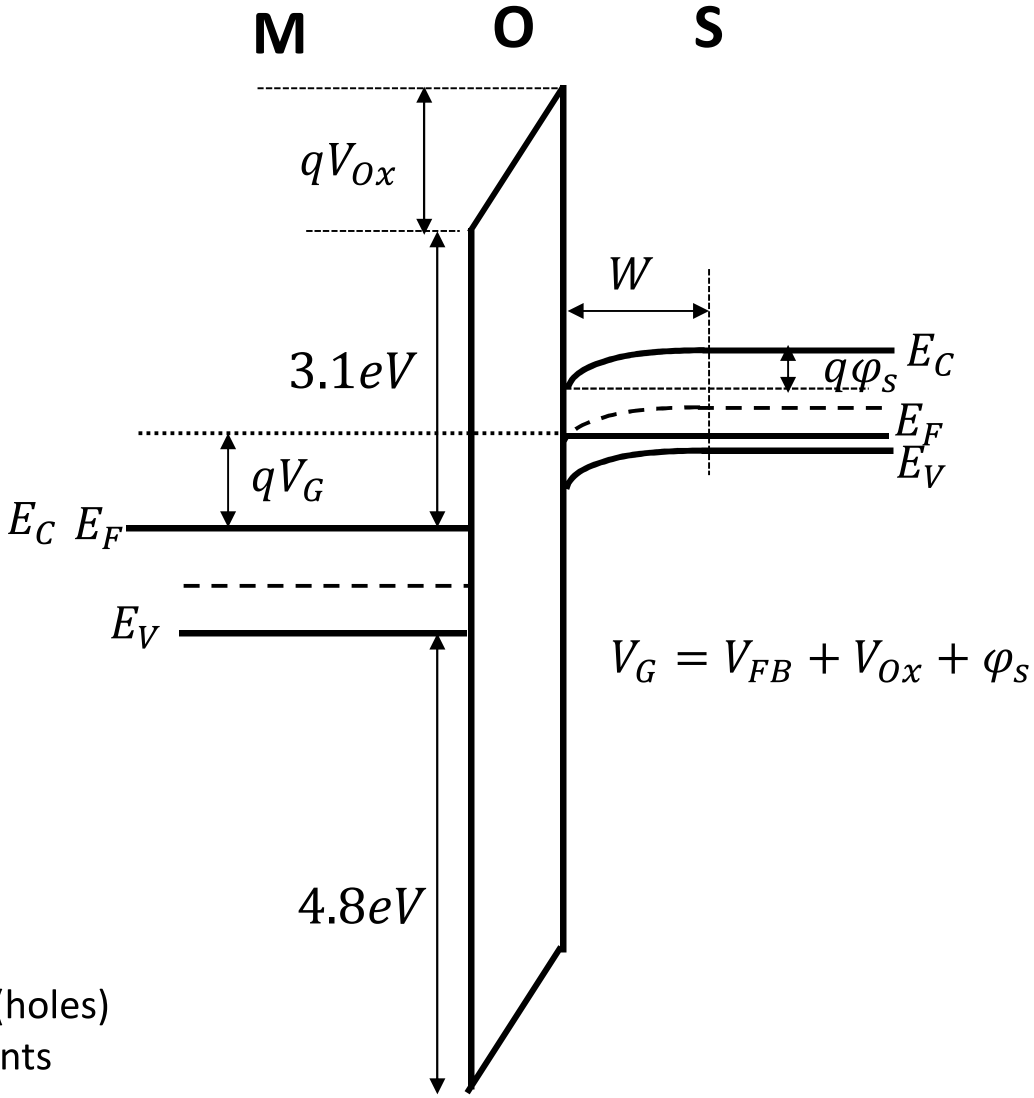
$V_G < V_{FB}$



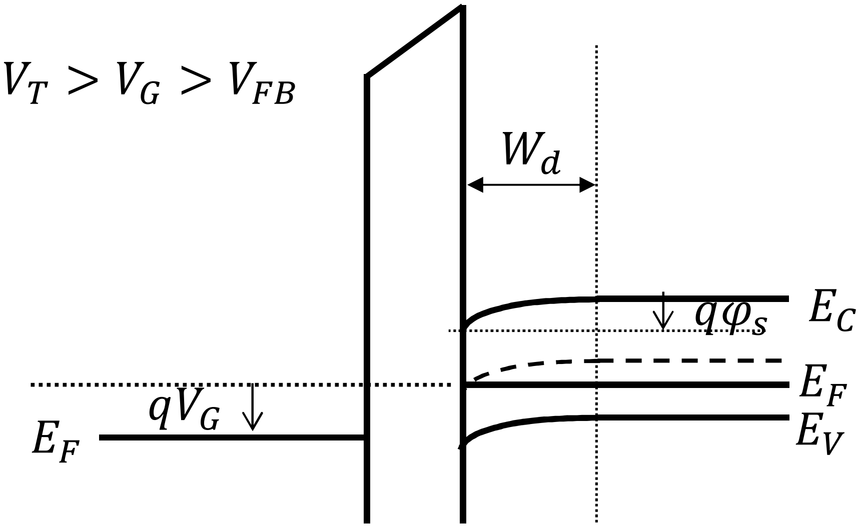


$$V_G = V_{FB} + V_{Ox} + \varphi_s$$

Si surface is depleted of mobile carriers (holes)
=> Surface charge is due to ionized dopants (acceptors)

Depletion (Weak Inversion)

$V_T > V_G > V_{FB}$



$$\frac{d\mathcal{E}}{dx} = \frac{-qN_A}{\epsilon_{Si}} = \frac{d^2\varphi}{dx^2} \quad \rightarrow \varphi_s = \frac{qN_A x^2}{2\epsilon_{Si}}$$

$$\rightarrow W_d = \sqrt{\frac{2\epsilon_{Si}}{qN_A}\varphi_s} \qquad V_{Ox} = \frac{-Q_{dep}}{C_{Ox}}$$

$$V_G = V_{FB} + V_{Ox} + \varphi_s \;\rightarrow\; V_G = V_{FB} + \varphi_s + \frac{1}{C_{Ox}}\sqrt{2qN_A\epsilon_{Si}\varphi_s}$$

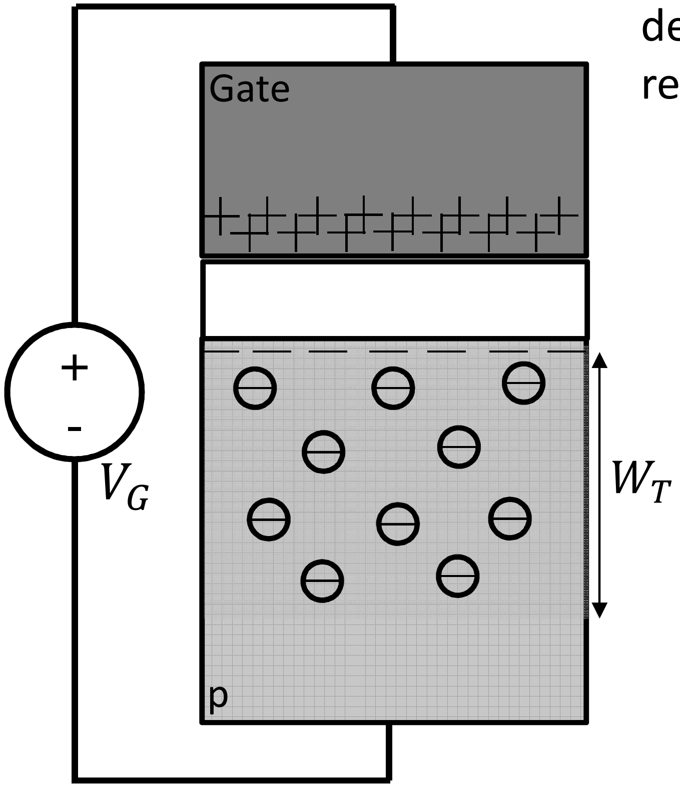
Solving for φ_s :

$$\varphi_s = \frac{qN_A\epsilon_{Si}}{2C_{Ox}^2}\left[\sqrt{1 + \frac{2C_{Ox}^2}{qN_A\epsilon_{Si}}(V_G - V_{FB})} - 1\right]^2$$

$$Q_{dep} = -qN_A W_d = -\sqrt{2qN_A\epsilon_{Si}\varphi_s}$$

Strong Inversion

$V_G > V_T$



Significant density of mobile electrons at surface (surface is n-type)

As V_G is increased above V_T, the negative charge in the Si is increased by adding mobile electrons (rather than by depleting the Si more deeply), so the depletion width remains ~ constant at $W = W_T$

$$\varphi_s \cong 2\varphi_F \qquad \rightarrow W \cong W_T = \sqrt{\frac{2\epsilon_{Si}}{qN_A}(2\varphi_F)}$$

$$V_G = V_{FB} + \varphi_s + V_{Ox}$$

$$= V_{FB} + 2\varphi_F - \frac{Q_{dep} + Q_{inv}}{C_{Ox}}$$

$$= V_{FB} + 2\varphi_F - \frac{\sqrt{2q\epsilon_{Si}N_A(2\varphi_F)}}{C_{Ox}} - \frac{Q_{inv}}{C_{Ox}}$$

$$V_G = V_T - \frac{Q_{inv}}{C_{Ox}}$$

$$\boxed{\therefore \quad Q_{inv} = -C_{Ox}(V_G - V_T)}$$

φ_s and W vs. V_G

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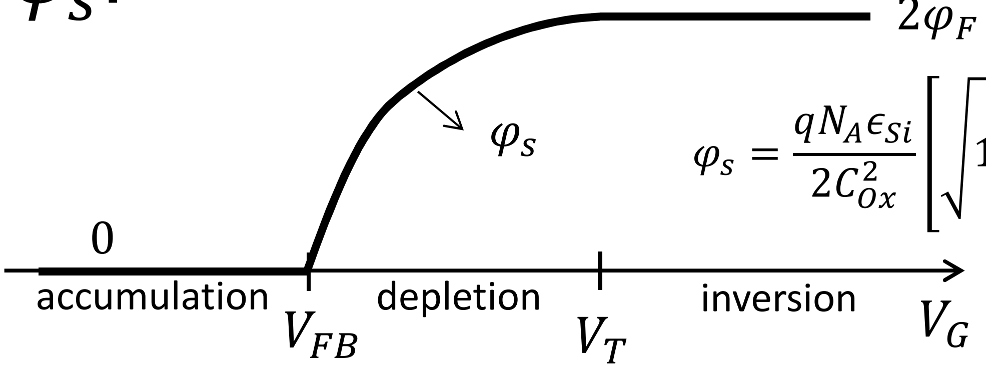
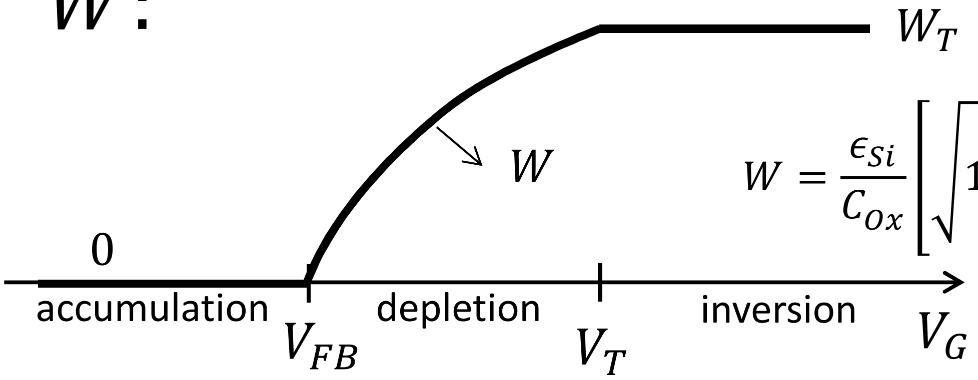
φ_S:



$$\varphi_s = \frac{qN_A\epsilon_{Si}}{2C_{Ox}^2}\left[\sqrt{1+\frac{2C_{Ox}^2}{qN_A\epsilon_{Si}}(V_G - V_{FB})} - 1\right]^2 \quad (V_{FB} < V_G < V_T)$$

W:



$$W_T = \sqrt{2\epsilon_{Si}(2\varphi_F)/qN_A}$$

$$W = \frac{\epsilon_{Si}}{C_{Ox}}\left[\sqrt{1+\frac{2C_{Ox}^2}{qN_A\epsilon_{Si}}(V_G - V_{FB})} - 1\right] \quad (V_{FB} < V_G < V_T)$$

Total Charge Density in Si, Q_S

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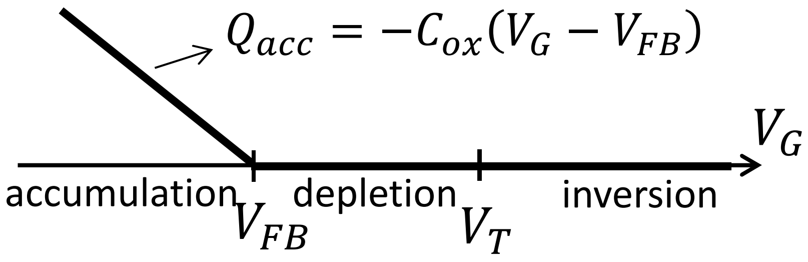
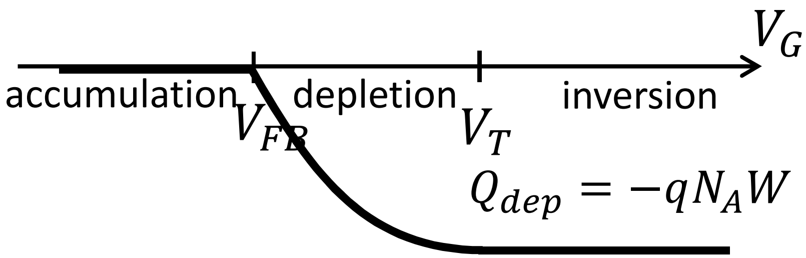
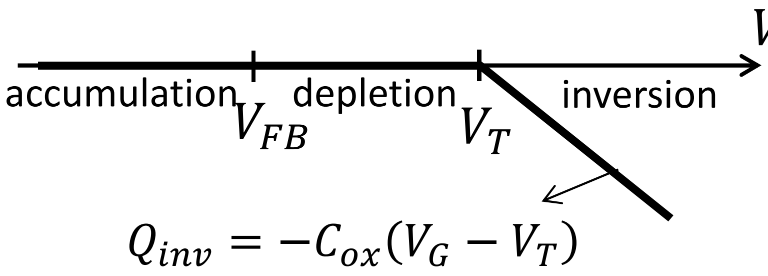
Q_{acc}:


$Q_{acc} = -C_{ox}(V_G - V_{FB})$

Q_{dep}:

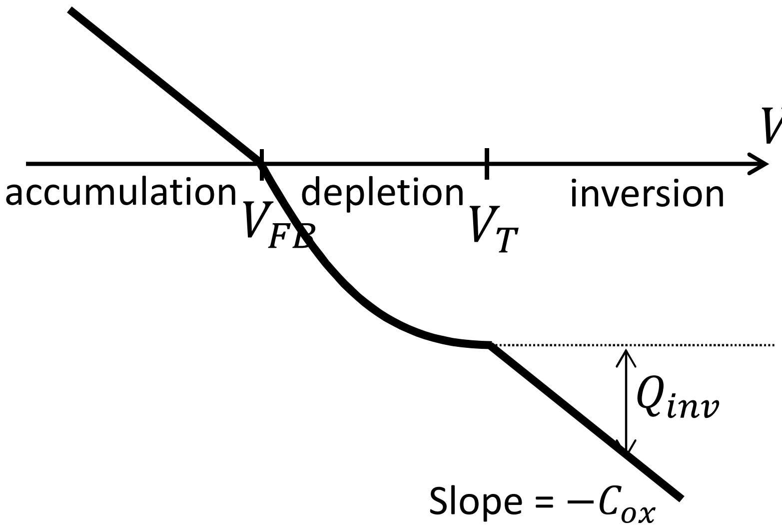

$Q_{dep} = -qN_AW$

Q_{inv}:

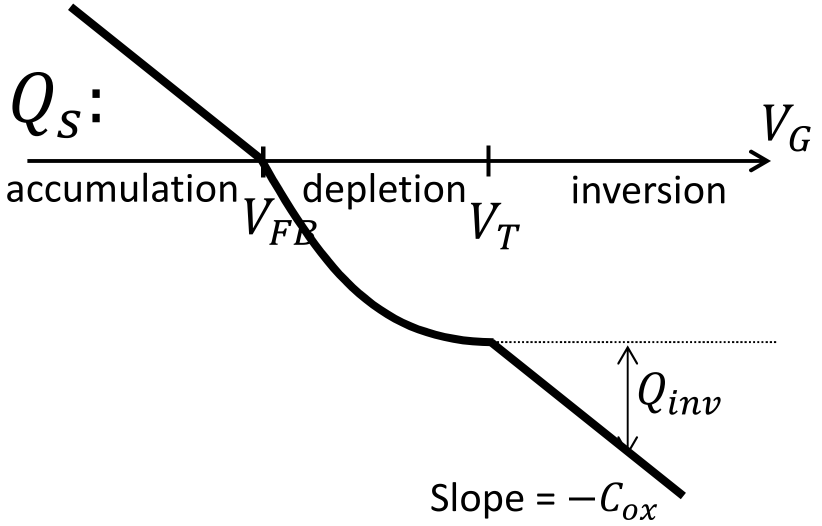

$Q_{inv} = -C_{ox}(V_G - V_T)$

$$Q_s = Q_{acc} + Q_{dep} + Q_{ivn}$$

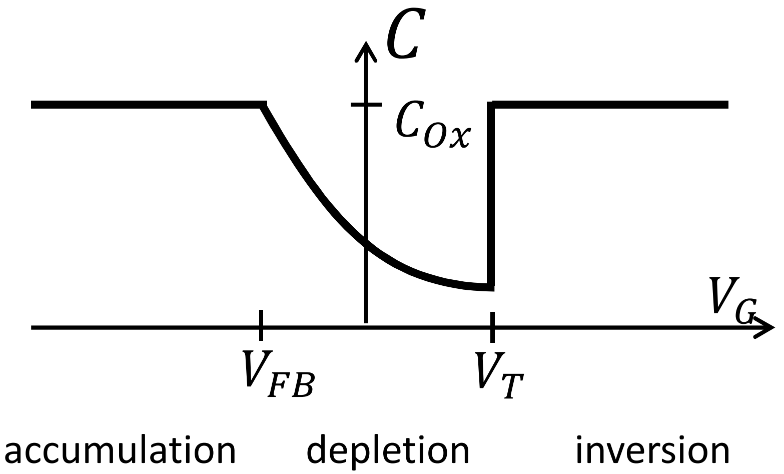
Q_s:



MOS C-V Characteristics

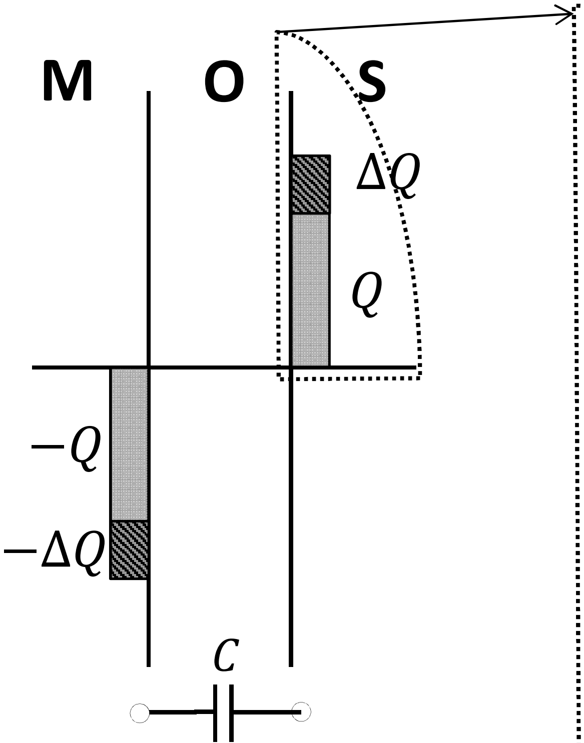


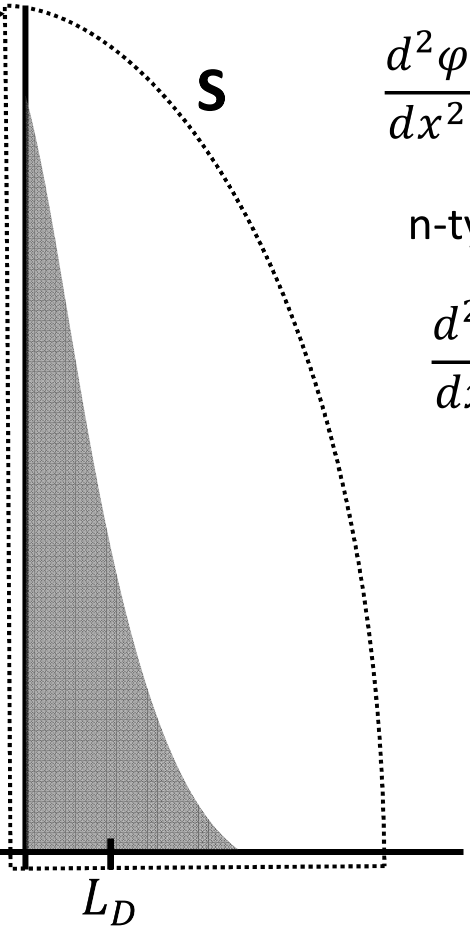
$$C = \left|\frac{dQ_{gate}}{dV_G}\right| = \left|\frac{dQ_s}{dV_G}\right|$$



Debye Length

- As the gate voltage is varied, incremental charge is added/subtracted to/from the gate and substrate.
- The incremental charges are separated by the gate oxide.





$$C = \left|\frac{dQ_{acc}}{dV_G}\right| = C_{Ox}$$

$$\frac{d^2\varphi}{dx^2} = -\frac{\rho}{\epsilon} = \frac{q}{\epsilon}(N_D - N_A + p - n)$$

n-type bulk: $\frac{d^2\varphi}{dx^2} = \frac{q}{\epsilon}(N_D - n)$

$$\frac{d^2\varphi}{dx^2} = \frac{q}{\epsilon}\left(N_D - n_i e^{-(\varphi_n - \varphi)/\varphi_{th}}\right)$$

$$= \frac{q}{\epsilon} N_D\left(1 - e^{\varphi/\varphi_{th}}\right)$$

$$\cong \frac{q}{\epsilon} N_D \frac{\varphi}{\varphi_{th}} = \frac{\varphi}{L_D^2}$$

$$L_D = \sqrt{\frac{\epsilon\, kT}{q^2 N_D}}$$

Flat-Band Capacitance

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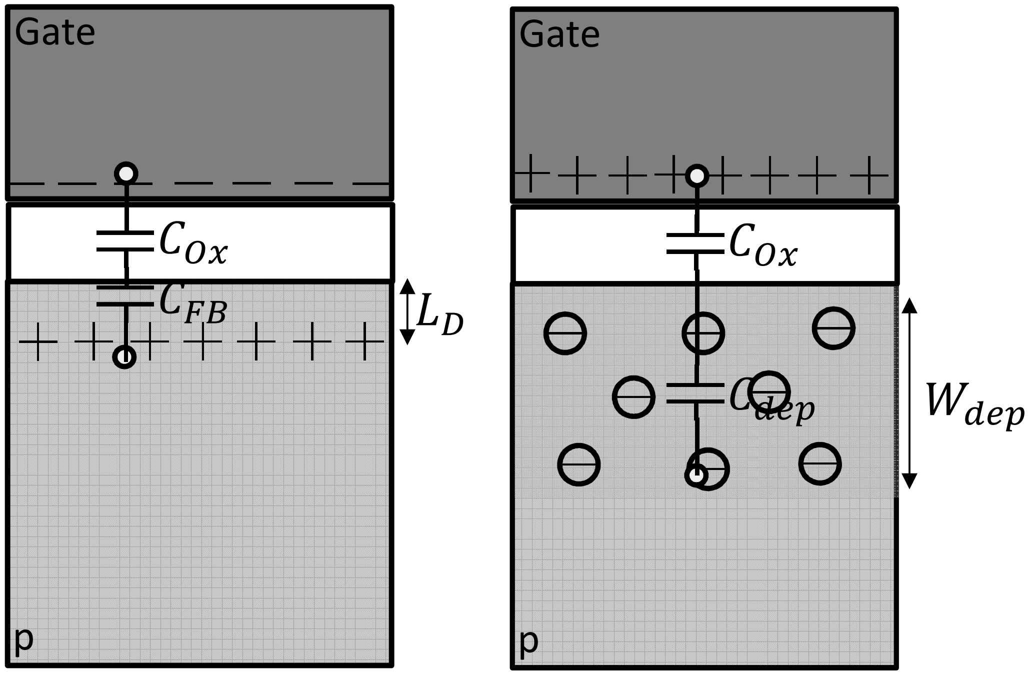
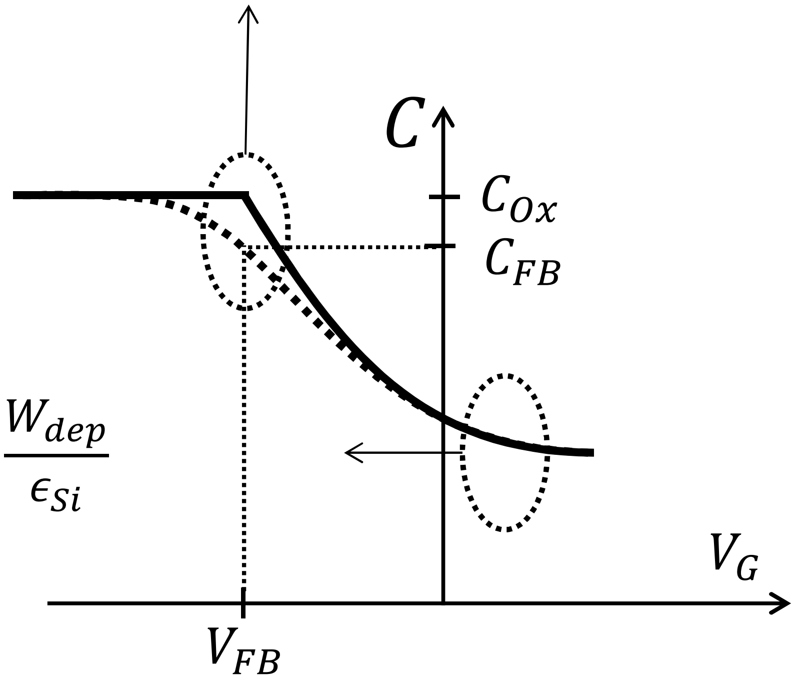


$$C_{FB} = \frac{C_{Ox} C_D}{C_{Ox} + C_D}$$

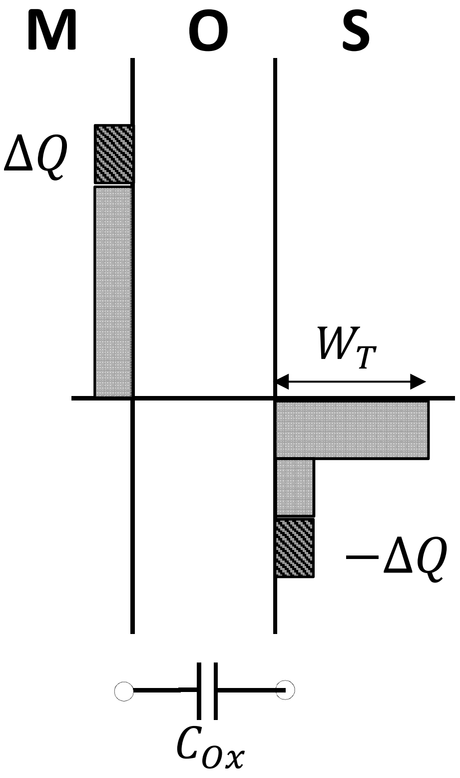
$$\rightarrow \frac{1}{C_{FB}} = \frac{t_{Ox}}{\epsilon_{Ox}} + \frac{L_D}{\epsilon_{Si}}$$



$$\frac{1}{C} = \frac{t_{Ox}}{\epsilon_{Ox}} + \frac{W_{dep}}{\epsilon_{Si}}$$

Capacitance in Inversion

CASE 1: Inversion-layer charge can be supplied/removed quickly enough to respond to changes in the gate voltage.



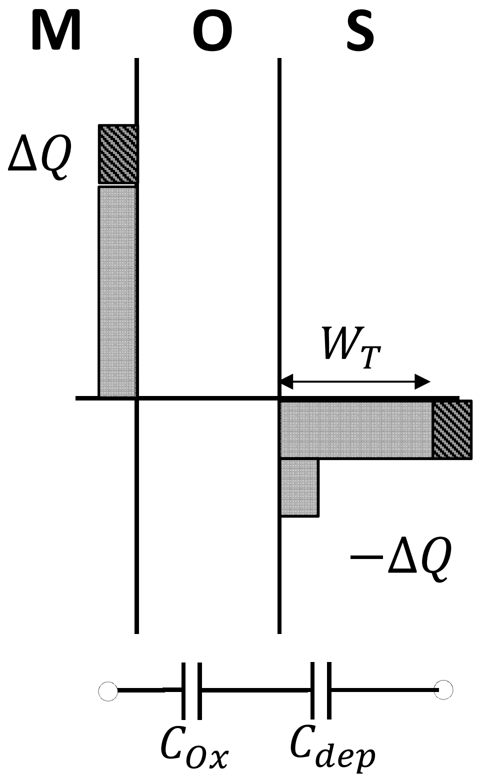
→ Incremental charge is effectively added/subtracted at the surface of the substrate.

Time required to build inversion-layer charge = $2N_A\tau_0/n_i$, where τ_0 = minority-carrier lifetime at the surface

$$C = \left|\frac{dQ_{inv}}{dV_G}\right| = C_{Ox}$$

Capacitance in Inversion

CASE 2: Inversion-layer charge *can not* be supplied/removed quickly enough to respond to changes in the gate voltage.



→ Incremental charge is effectively added/subtracted at depth WT in the substrate.

$$\frac{1}{C} = \frac{1}{C_{Ox}} + \frac{1}{C_{dep}}$$

$$= \frac{1}{C_{Ox}} + \frac{W_T}{\epsilon_{Si}}$$

$$= \frac{1}{C_{Ox}} + \sqrt{\frac{2(2\varphi_F)}{qN_A\epsilon_{Si}}} \equiv \frac{1}{C_{min}}$$

Supply of Inversion Charge

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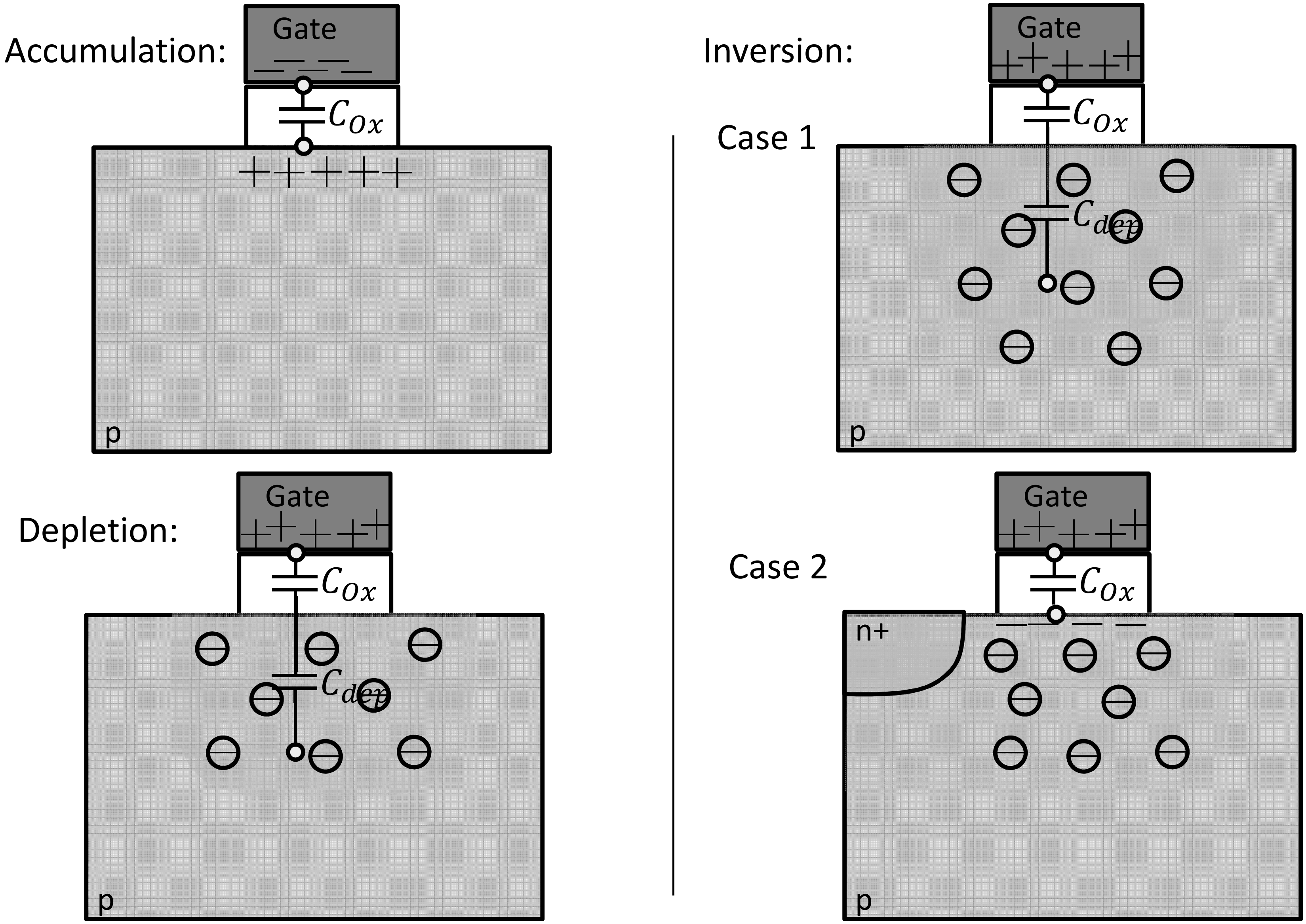
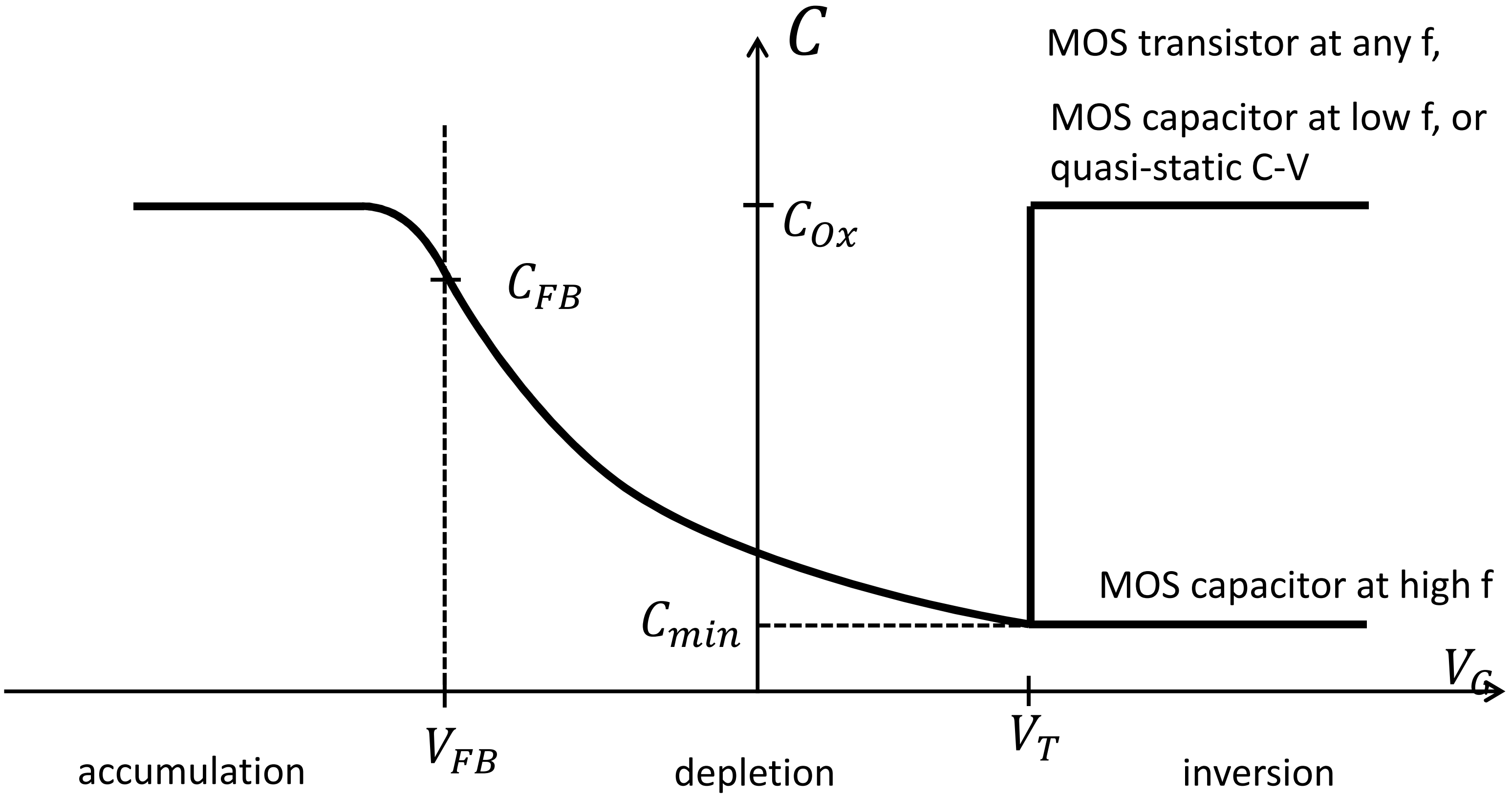


Boundary Condition

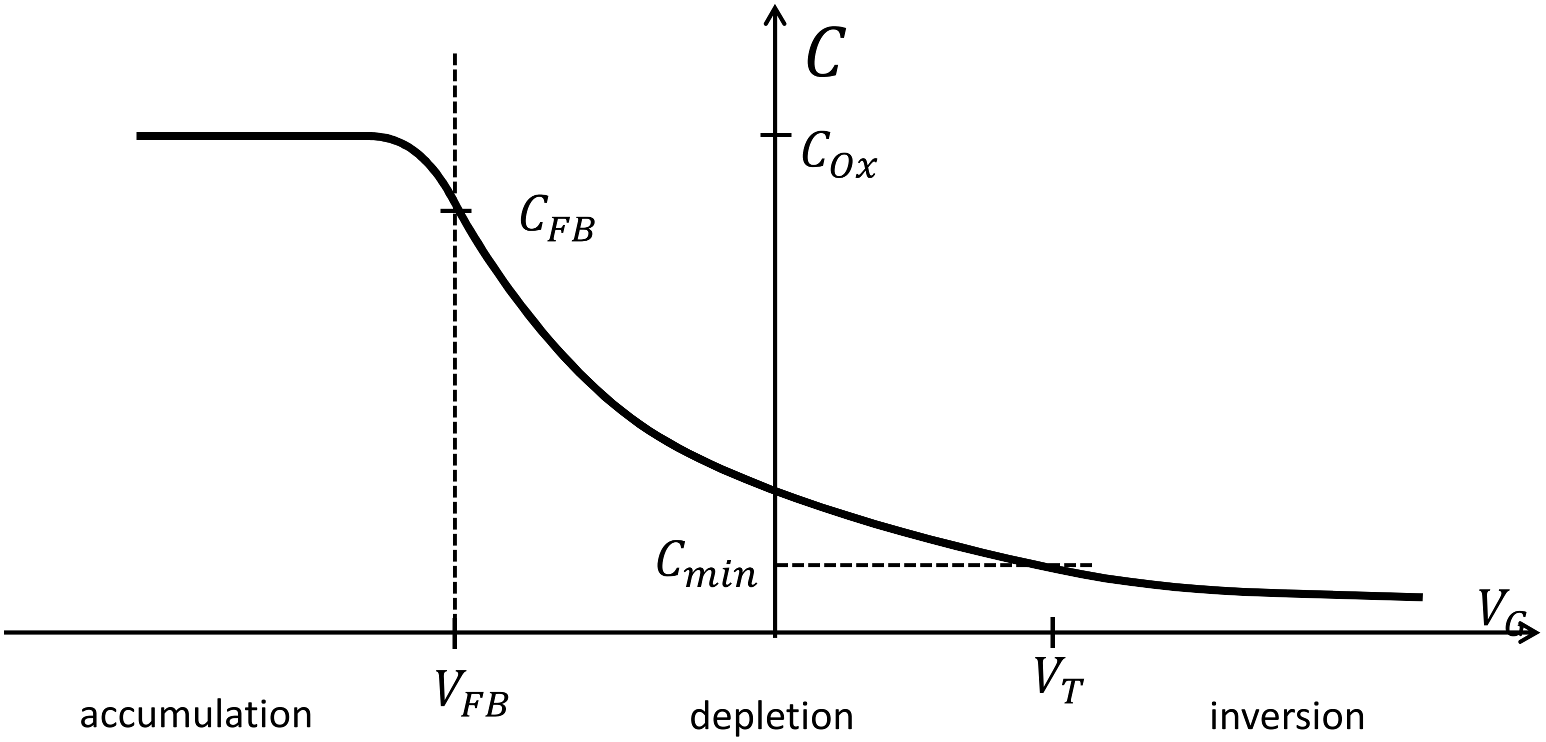


Deep Depletion

If V_G is scanned quickly, Q_{inv} cannot respond to the change in V_G. The increase in substrate charge density Q_s must then come from an increase in depletion charge density Q_{dep}

⇒ depletion depth W increases as V_G increases

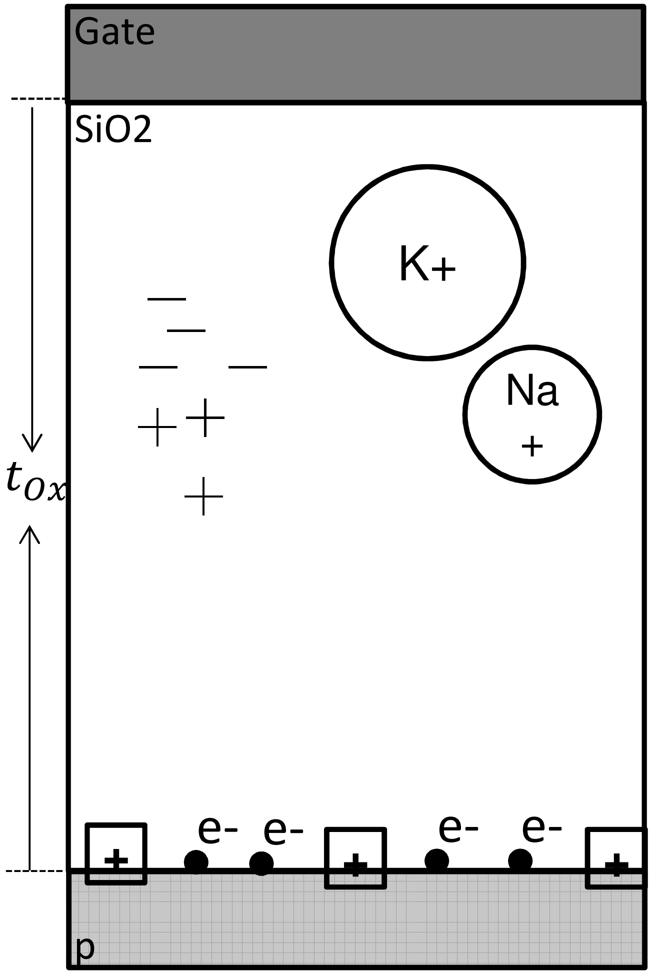
⇒ C decreases as V_G increases



Boundary Condition

Oxide Charges

In real MOS devices, there is always some charge in the oxide and at the Si/oxide interface.



In the oxide:

1. Trapped charge Qox
High-energy electrons and/or holes injected into oxide

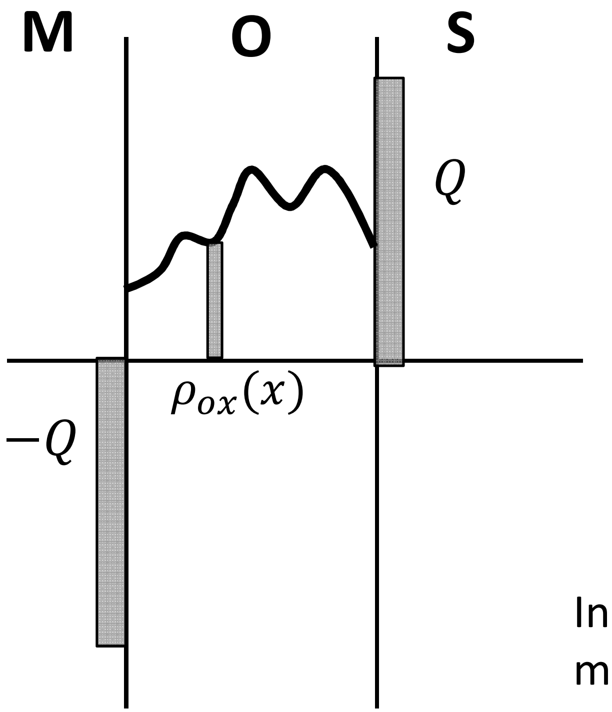
2. Mobile charge QM
Alkali-metal ions, which have sufficient mobility to drift in oxide under an applied electric field

At the interface:

1. Fixed charge QF
Excess Si (+)

2. Trapped charge QIT
Dangling bonds

Effect of Oxide Charges



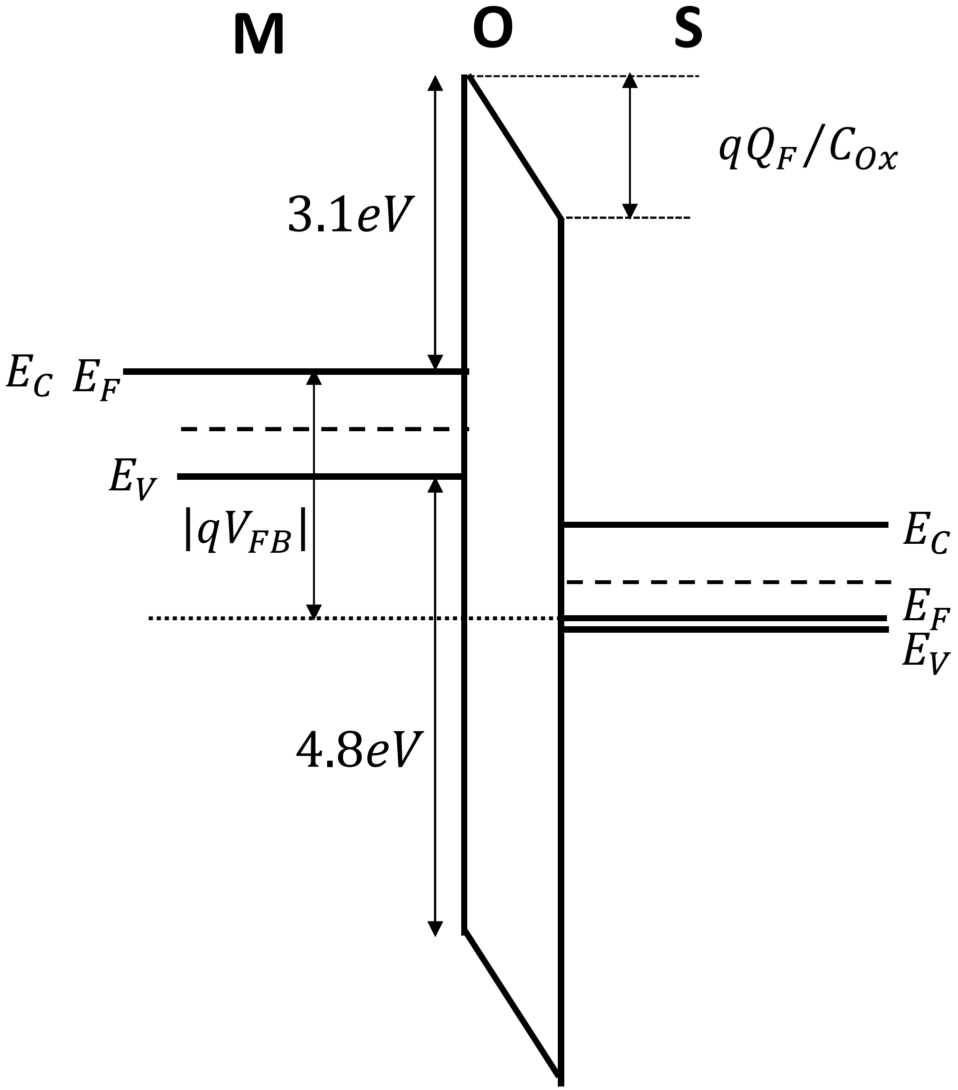
In general, charges in the oxide cause a shift in the gate voltage required to reach the threshold condition:

$$\Delta V_T = -\frac{1}{\epsilon_{SiO_2}} \int_0^{t_{Ox}} x\rho_{0x}(x)dx$$

(x defined to be 0 at metal-oxide interface)

In addition, they may alter the field-effect mobility of mobile carriers (in a MOSFET) due to Coulombic scattering

Fixed Oxide Charges Q_F



$$V_{FB} = \varphi_{ms} - \frac{Q_F}{C_{Ox}}$$

Parameter Extraction from C-V

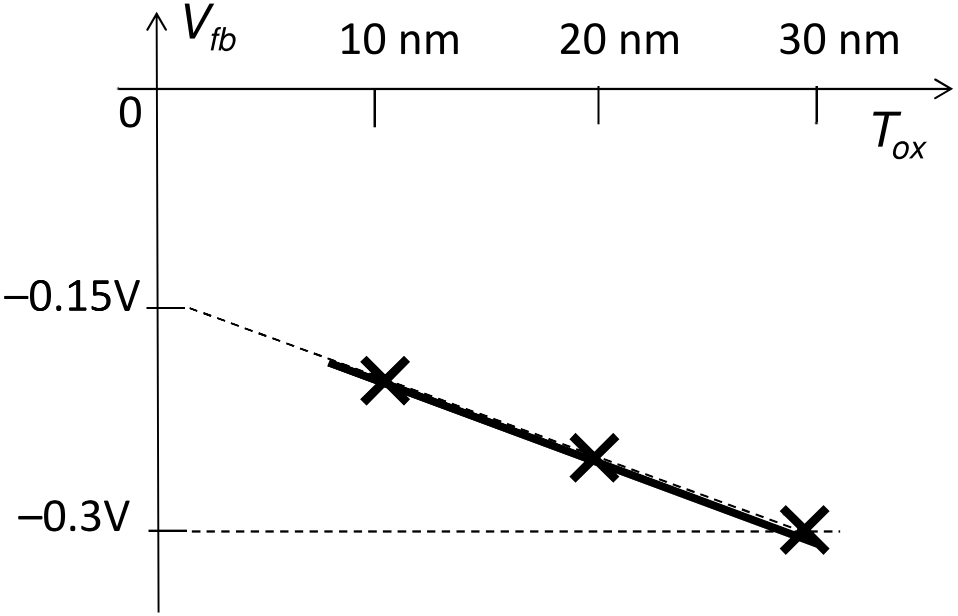
From a single C-V measurement, we can extract much information about the MOS device.

Suppose we know that the gate-electrode material is heavily doped n-type poly-Si (φ_M=4.05eV), and that the gate dielectric is SiO2 ($\epsilon_r = 3.9$):

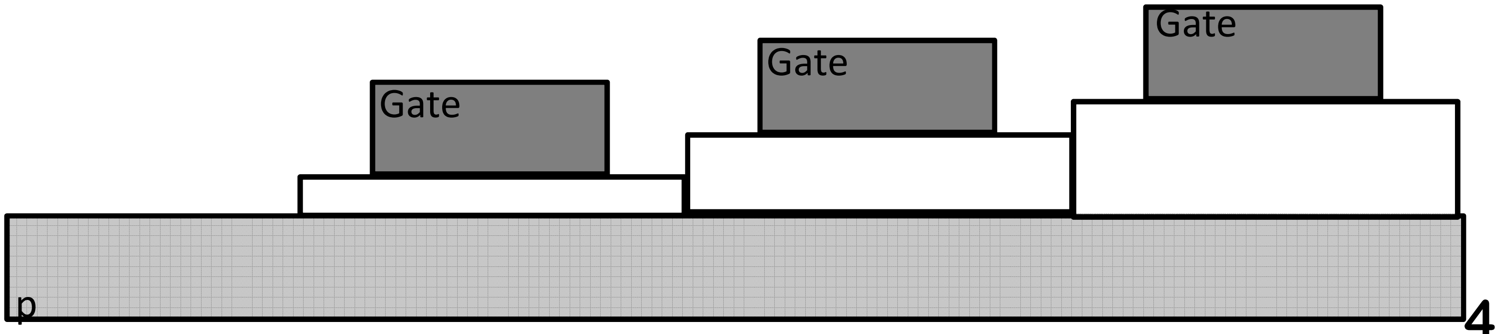
- ○ From $C_{max} = C_{Ox}$ we determine the oxide thickness x_0
- ○ From C_{min} and C_{Ox} we determine substrate doping (by iteration)
- ○ From substrate doping and C_{Ox} we calculate the flat-band capacitance C_{FB}
- ○ From the C-V curve, we can find
- ○ From φ_M, φ_S, C_{Ox}, and V_{FB} we can determine Q_F

Determination of φ_M and Q_F

Measure C-V characteristics of capacitors with different oxide thicknesses.
Plot V_{FB} as a function of x_0:

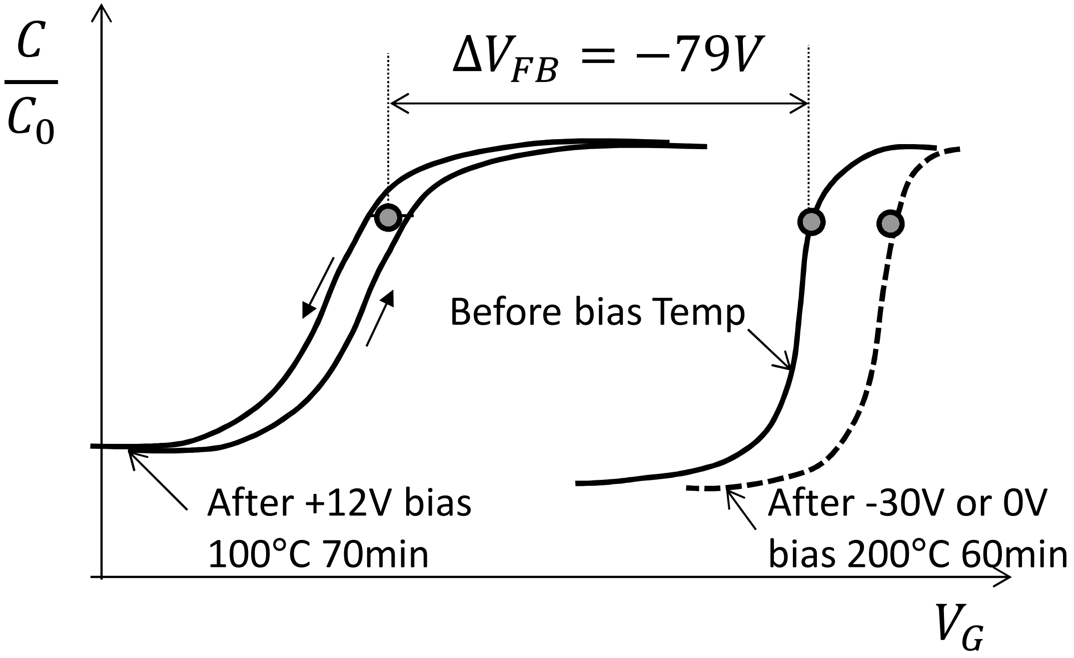


$$V_{FB} = \varphi_{ms} - \frac{Q_F}{\epsilon_{SiO_2}} t_{Ox}$$



Mobile Ions

Odd shifts in C-V characteristics were once a mystery:



$$\Delta V_{FB} = -\frac{Q_M}{C_{Ox}}$$

Source of problem: Mobile charge moving to/away from interface, changing charge centroid

Interface Traps

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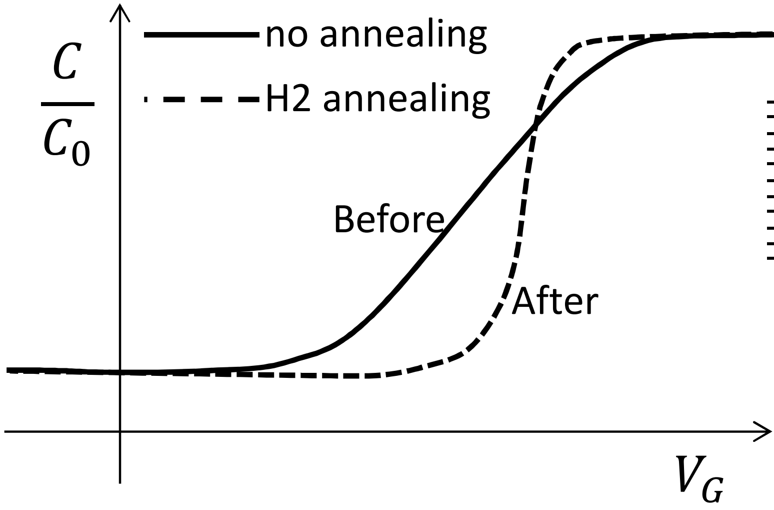
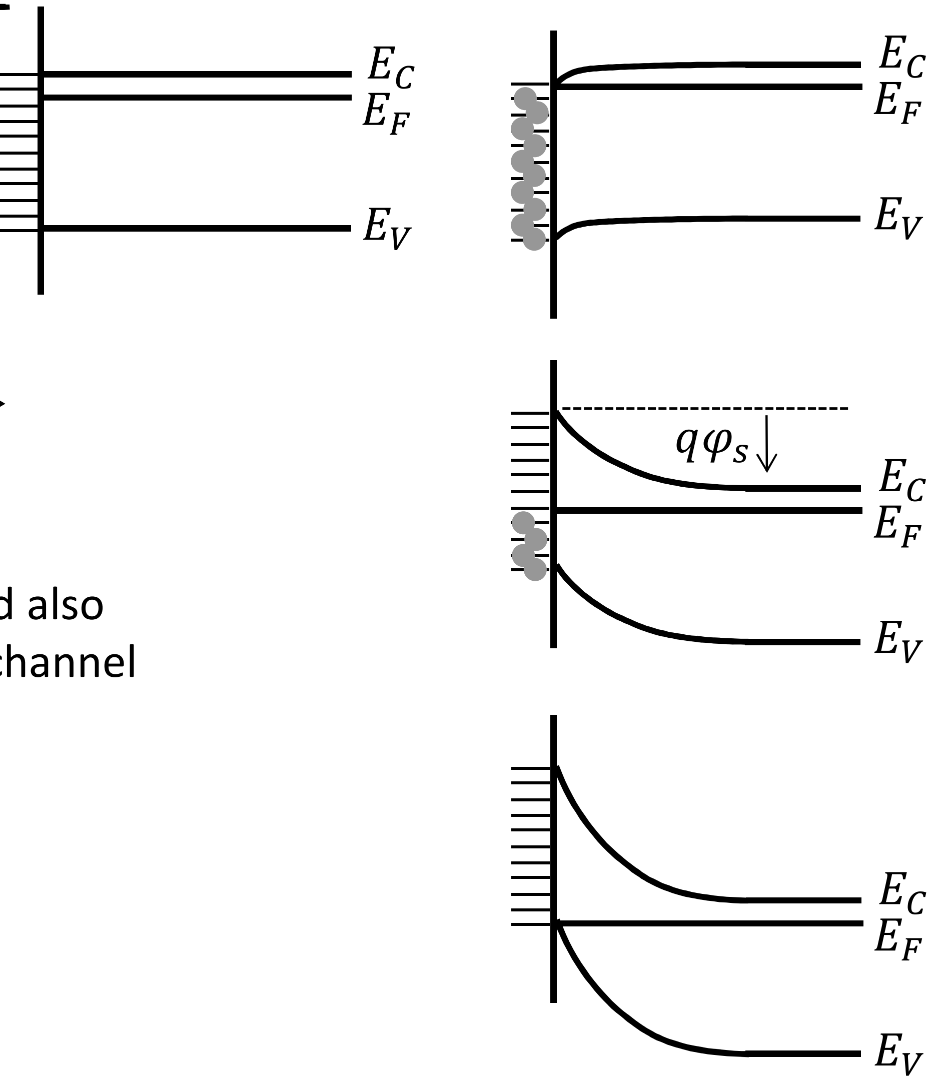


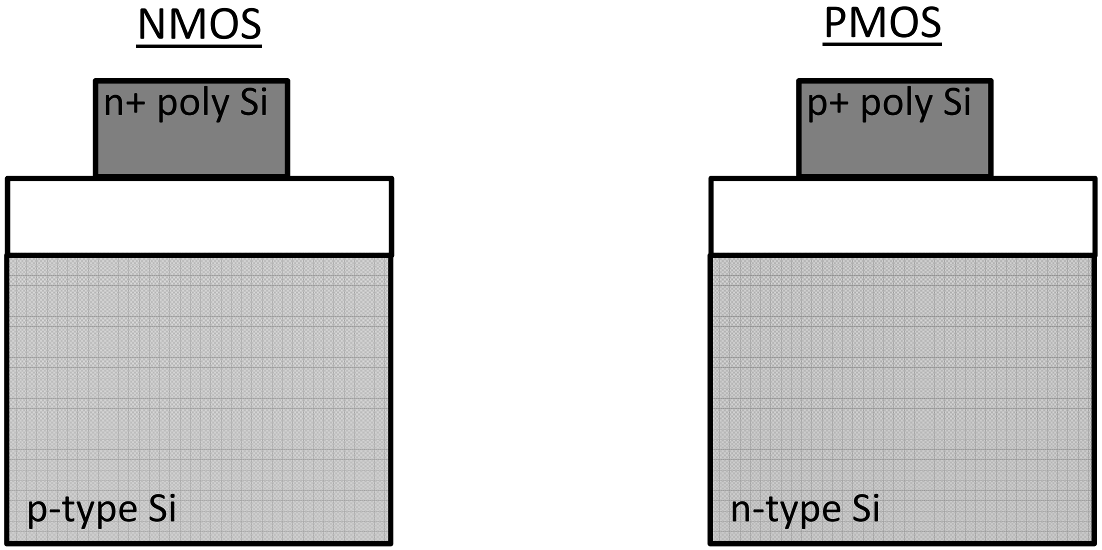


Traps cause “sloppy” C-V and also greatly degrade mobility in channel

$$\Delta V_G = -\frac{Q_{IT}(\varphi_s)}{C_{Ox}}$$

Poly-Si Gate Depletion

A heavily doped film of polycrystalline silicon (poly-Si) is typically employed as the gate-electrode material in modern MOS devices.


NMOS

PMOS

There are practical limits to the electrically active dopant concentration (usually less than $1\text{x}10^{20}$ cm^{-3})

⇒ The gate must be considered as a semiconductor, rather than a metal

MS Junction (Poly Gate)

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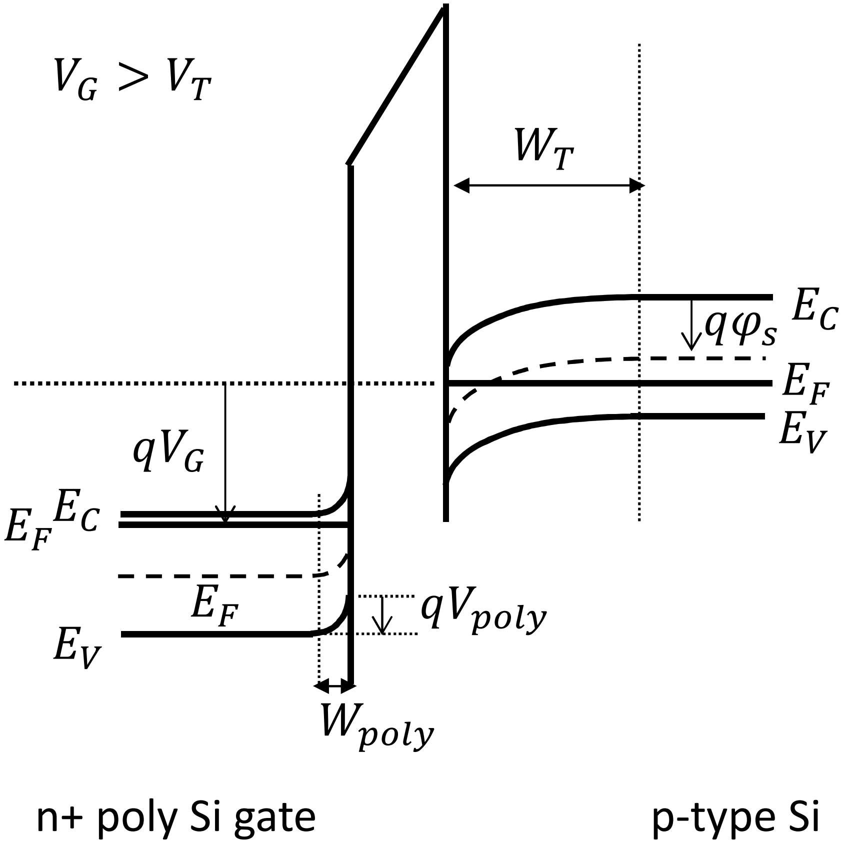
Si biased to inversion:



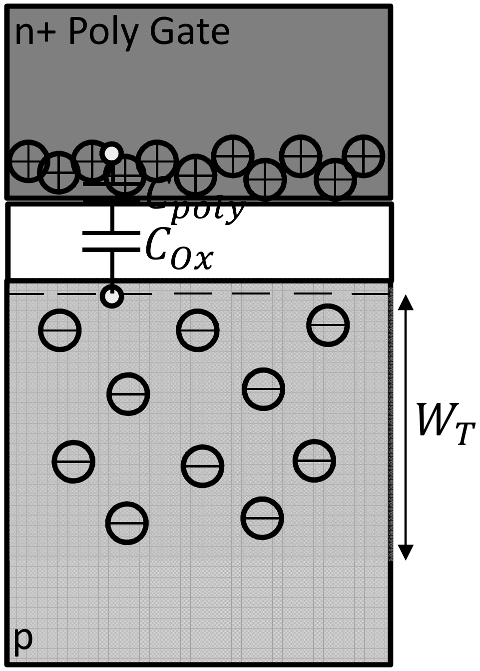
V_G is effectively reduced:

$$Q_{inv} = C_{Ox}\left(V_G - V_{poly} - V_T\right)$$

$$W_{poly} = \sqrt{\frac{2\epsilon_{Si} V_{poly}}{qN_{poly}}}$$

How can gate depletion be minimized?

Gate Depletion Effect



Gauss's Law dictates:

$$W_{poly} = \frac{\epsilon_{Ox}\mathcal{E}_{Ox}}{qN_{poly}}$$

t_{Ox} is effectively increased:

$$C = \left(\frac{1}{C_{Ox}} + \frac{1}{C_{poly}}\right)^{-1} = \left(\frac{t_{Ox}}{\epsilon_{SiO_2}} + \frac{W_{poly}}{\epsilon_{Si}}\right)^{-1}$$

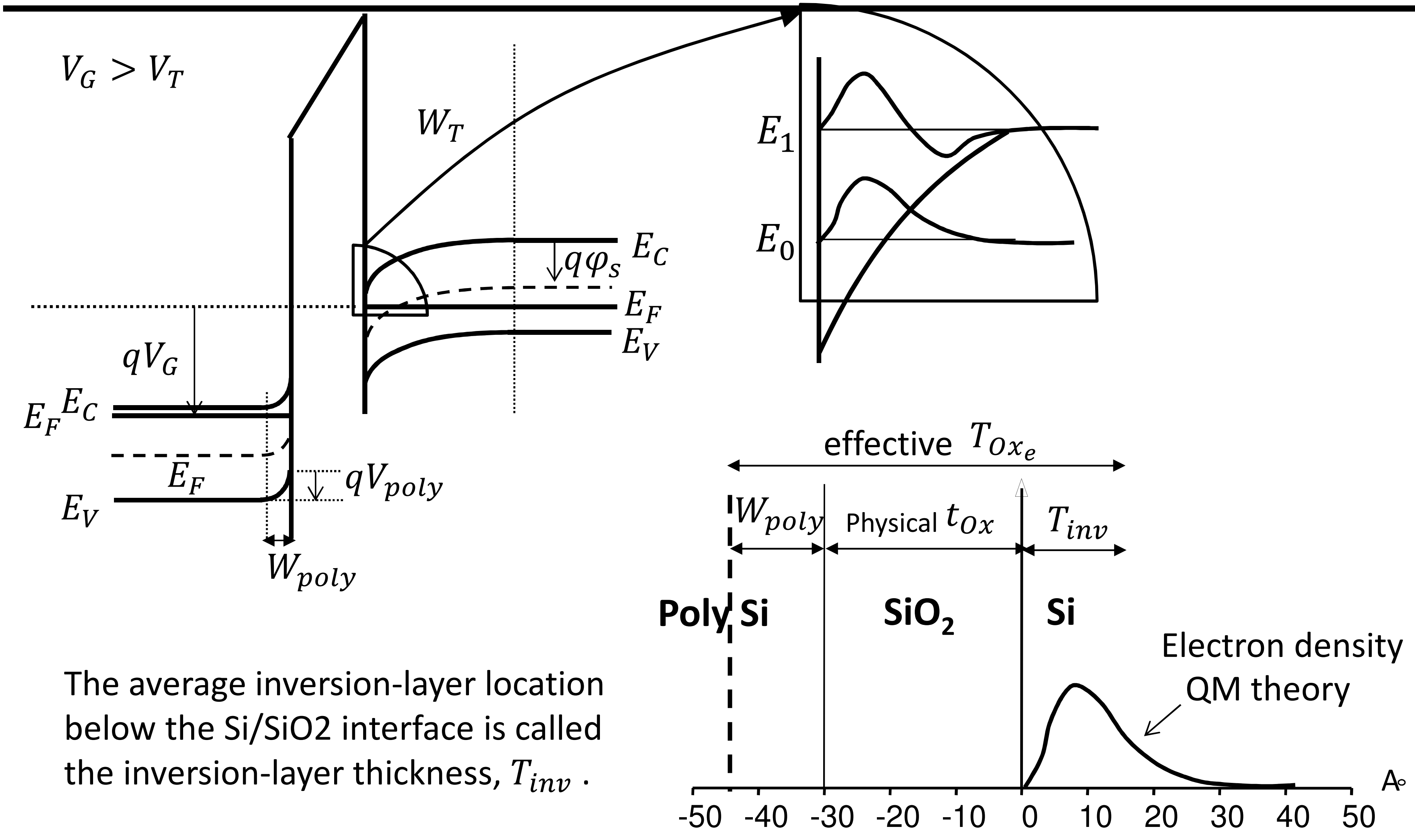
$$= \frac{\epsilon_{SiO_2}}{t_{Ox} + \frac{1}{3}W_{poly}}$$

$$Q_{inv} = C_{Ox}\left(V_G - V_{poly} - V_T\right)$$

$$Q_{inv} = \frac{\epsilon_{SiO_2}}{t_{Ox} + \frac{1}{3}W_{poly}}(V_G - V_T)$$

Inversion Layer Thickness T_{inv}

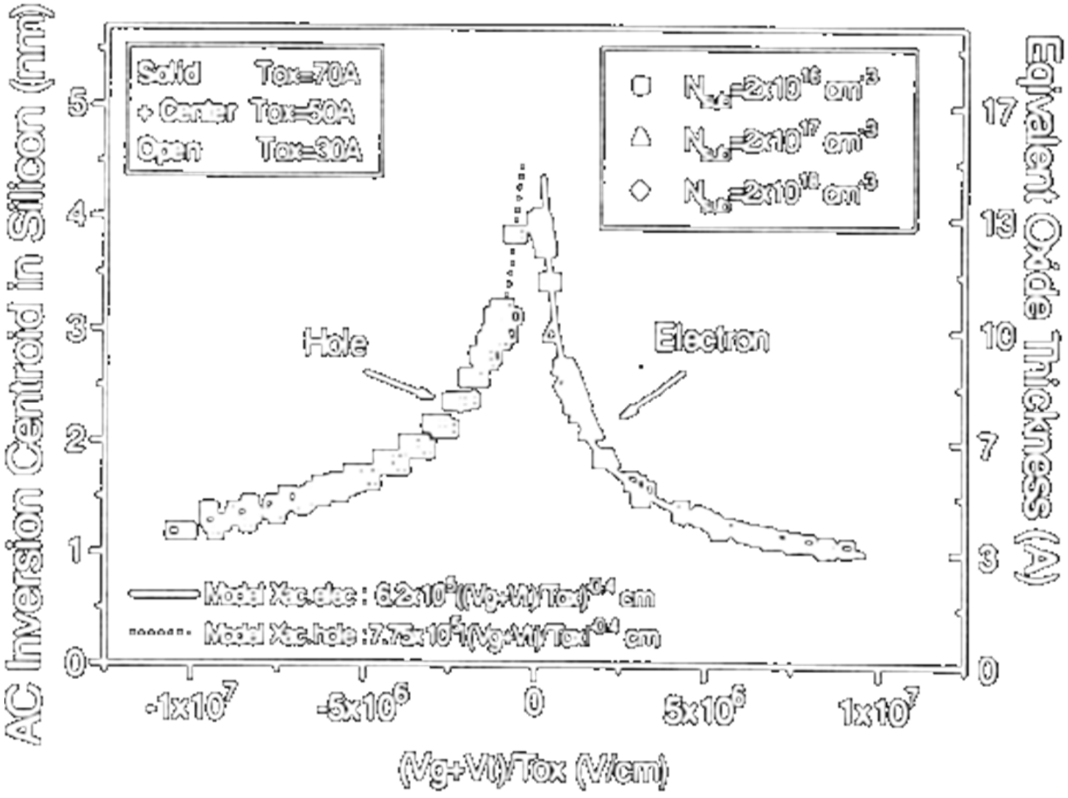
1.
2.
3.
4.
5.



The average inversion-layer location below the Si/SiO2 interface is called the inversion-layer thickness, T_{inv} .

Effective Oxide Thickness , T_{Oxe}

$$T_{Ox_e} = t_{Ox} + \frac{1}{3}W_{poly} + \frac{1}{3}T_{inv} \qquad @\, V_G = V_{DD}$$



$(V_G + V_T)/T_{Ox}$ can be shown to be the average electric field in the inversion layer. Tinv of holes is larger than that of electrons because of the difference in effective masses.

Effective Oxide Capacitance , C_{Oxe}

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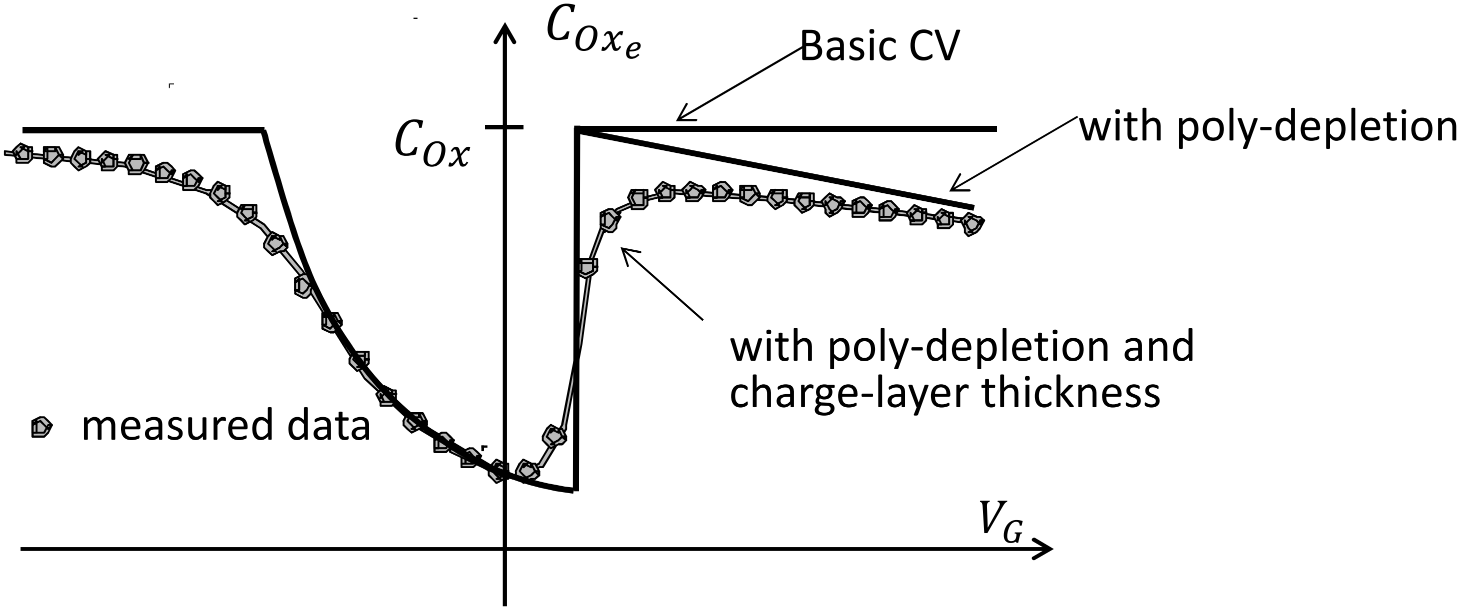
3. □□□□□□□
4. □□□□
5. □□□□□

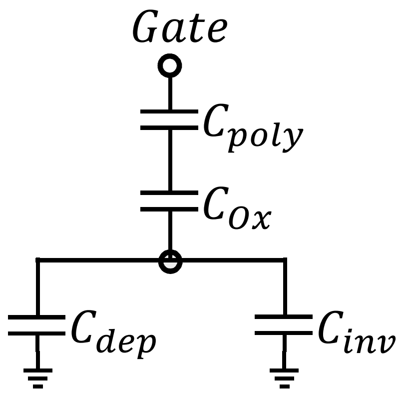
$$Q_{inv} = C_{Ox_e}(V_G - V_T)$$

$$T_{Ox_e} = t_{Ox} + \frac{1}{3}W_{poly} + \frac{1}{3}T_{inv}$$

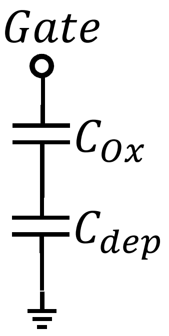


MOS Cap:
Equivalent Circuit in Depletion & Inversion

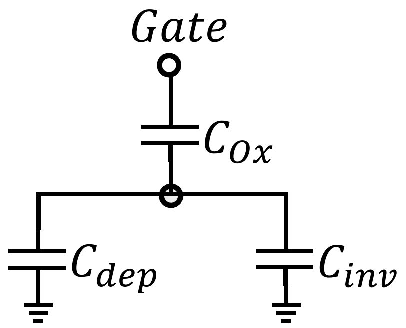
General case for both depletion and inversion regions.



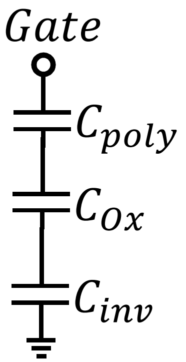
In the depletion regions



$V_G \approx V_T$



Strong inversion



V_T Adjustment by Ion Implantation

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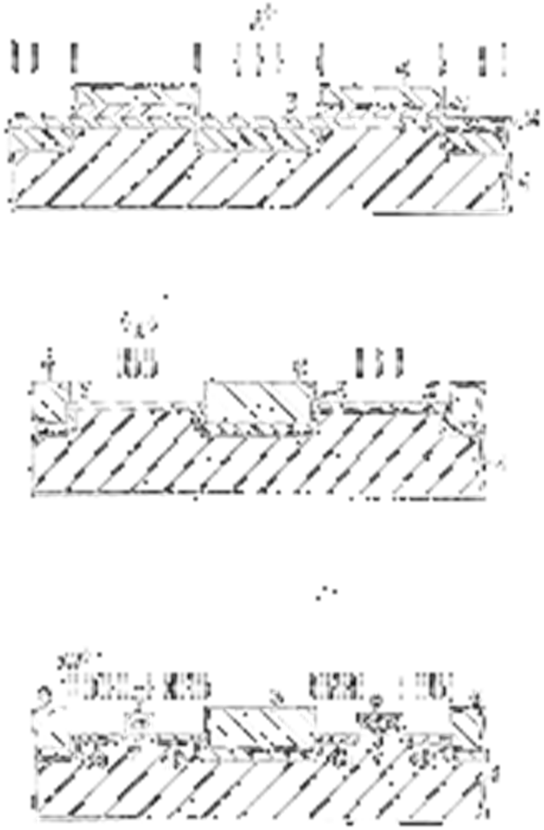
In modern IC fabrication processes, the threshold voltages of MOS transistors are adjusted by ion implantation:

- A relatively small dose NI (units: ions/cm2) of dopant atoms is implanted into the near-surface region of the semiconductor
- When the MOS device is biased in depletion or inversion, the implanted dopants add to the dopant-ion charge near the oxide-semiconductor interface.



$$\Delta V_T = -\frac{qN_I}{C_{Ox}}$$

$N_I > 0$ for donor atoms

$N_I < 0$ for acceptor atoms

Dynamic V_T Adjustment Bulk Voltage

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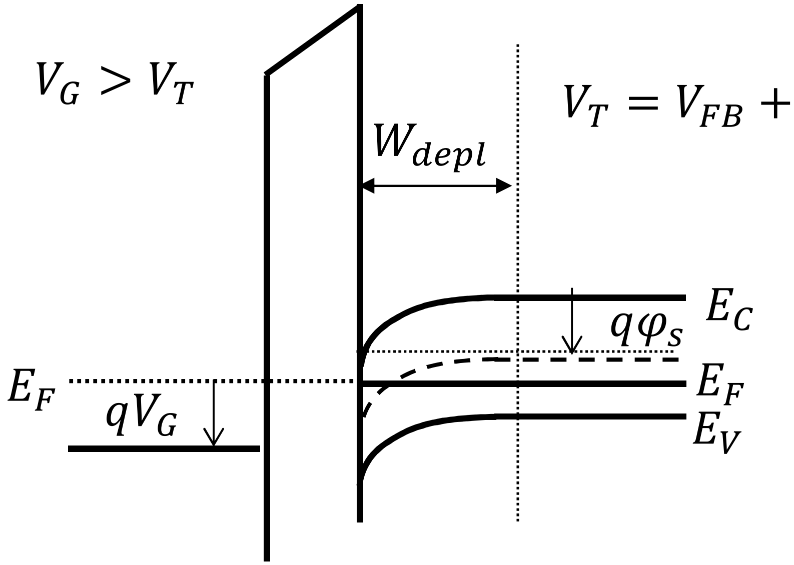
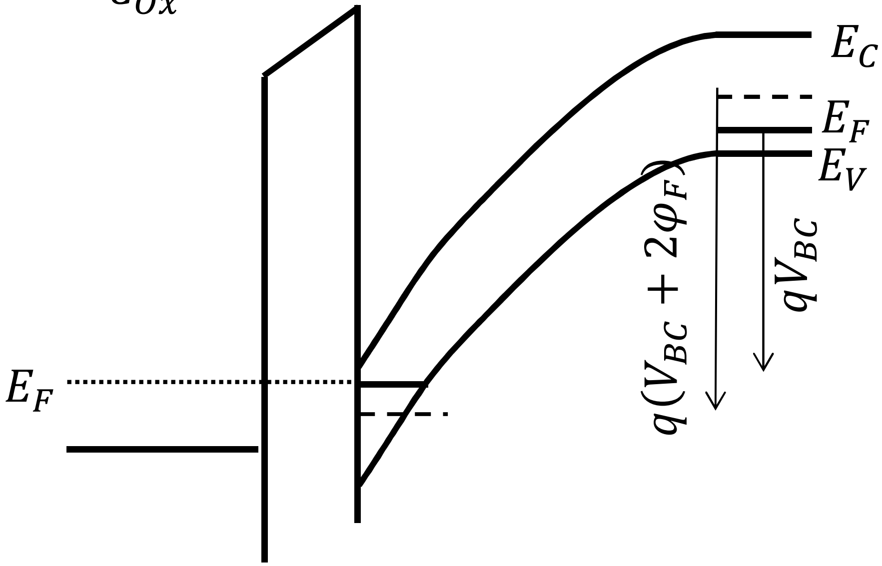
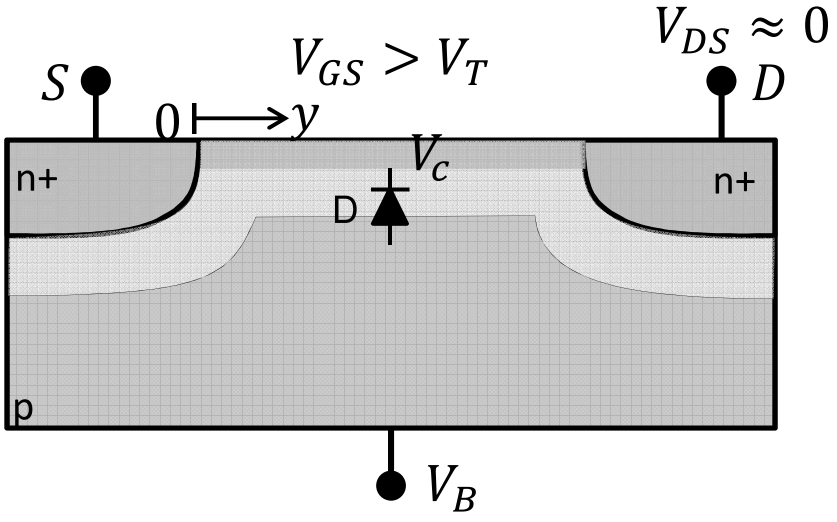


$$V_T = V_{FB} + 2\varphi_F + \frac{Q_{depl}}{C_{Ox}}$$





$$V_T = V_{FB} + V_C + 2\varphi_F + \frac{Q_{depl}}{C_{Ox}}$$

$$Q_{depl} = \sqrt{2qN_A\epsilon_{Ox}(V_{BC} + 2\varphi_F)}$$

CCD Imager and CMOS Imager

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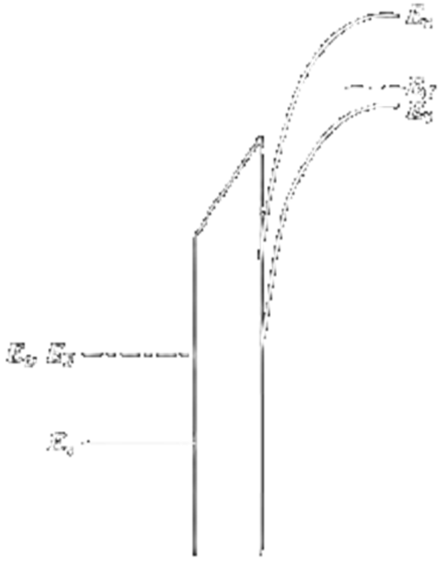
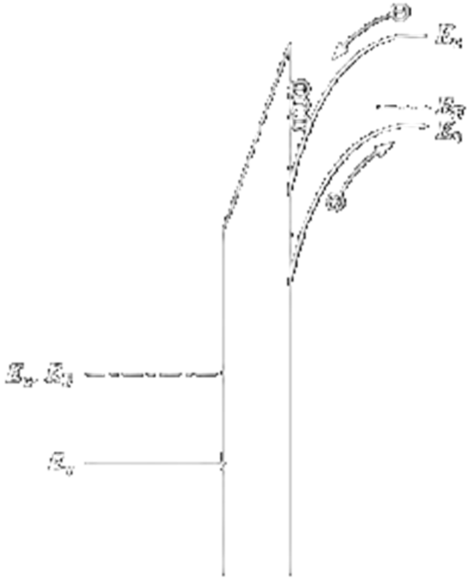


Deep depletion, Q_{inv}= 0



Exposed to light