Efficient Coupled Noise Estimation for On-Chip Interconnects

Anirudh Devgan
Austin Research Laboratory
IBM Research Division, Austin TX 78758
devgan@austin.ibm.com

Abstract

Noise analysis and avoidance is an increasingly critical step in deep submicron design. Ever increasing requirements on performance have led to widespread use of dynamic logic circuit families and its other derivatives. These aggressive circuit families trade off noise margin for timing performance making them more susceptible to noise failure and increasing the need for noise analysis. Currently, noise analysis is performed either through circuit or timing simulation or through model order reduction. These techniques in use are still inefficient for analyzing massive amount of interconnect data found in present day integrated circuits. This paper presents efficient techniques for estimation of coupled noise in on-chip interconnects. This noise estimation metric is an upper bound for RC circuits, being similar in spirit to Elmore delay in timing analysis. Such an efficient noise metric is especially useful for noise criticality pruning and physical design based noise avoidance techniques.

1. Introduction

Timing and power analysis have always been critical in the design process. With increasing operating frequencies, noise analysis and avoidance is becoming equally important, or in some cases, more important than timing and power analysis. Advances in process technology allow shrinking of the minimum distance between adjacent wires. This has led to increase in the coupling capacitance from a net to its neighbors. Furthermore, the distance between two wires can be reduced more than the height of the wire itself. The thickness of the wire is typically greater than its width, causing an increase in ratio of coupling capacitance to the total capacitance. For present day processes, the ratio of coupling capacitor to the grounded capacitor can be as high as 35%. Due to the increase in the coupling capacitance, a switching net can electrical affect its neighboring nets. If the neighboring net is quiet, this capacitive coupling induces a noise pulse which can have a detrimental effect on the circuit response.

The criticality of the noise analysis problem is also dependent on the type of logic circuits used in the design. Some logic circuits are more susceptible to noise than others. Over the last several years, dynamic logic circuit families and its derivatives have gained wide spread acceptance. Dynamic circuits use a clock signal or clock-like signal to precharge the output voltage. The circuit is then evaluated by a N-tree structure. The advantage of dynamic logic is that the capacitive load on the previous stage is reduced. The previous stage has to drive the capacitance of only the NMOS transistor, as compared to the capacitance of both the NMOS and PMOS transistors in CMOS logic. However, the switching point of dynamic logic gates is the threshold voltage of the NMOS transistor, rather than typically half of the supply voltage for CMOS. Hence, dynamic logic circuits trade noise margin to reduce the circuit delay. This reduced noise margin and increased noise susceptibility mandates greater use of noise analysis. The problem of noise failure can be more severe than the problem of timing failure. For most circuits, timing failure can be recovered by increasing the clock speed and thus allowing more time for signal propagation. However, noise is caused by, among other things, capacitive coupling and input slope, which are much more difficult to control from the chip terminals. For example, changing the capacitive coupling normally requires rewiring the chip. If the noise problem goes undetected to fabrication, correcting it may cause an expensive second fabrication run.

Various transient analysis techniques can be used to estimate noise. Circuit or timing simulation techniques, like SPICE[3], can be used. In cases when the problem can be modeled as a linear circuit (which it can be for most coupled noise problems), specialized linear model reduction techniques [4][5] are typically used[2]. Model reduction helps in reducing the computational cost, but in several cases, the cost is still unacceptable given the enormous complexity of interconnects. Using modern moment matching methods, it may still require more than a day to compute the noise in a modern microprocessor. The constrains on efficiency are even greater if noise analysis is to be used within a physical design system. Most of the current physical design systems use a geometric model for noise (e.g based on geometric distance between wires, etc.). However, these simple formulae do not have an electrical and circuit theoretic formulation and are hence inaccurate. And use of accurate moment matching or simulation techniques is often inefficient, both for noise verification and noise avoidance. Hence, a more efficient electric metric for noise analysis is needed to address these requirements.

This paper presents an electrical metric for efficiently estimating the coupled noise for on-chip interconnects. It determines the maximum noise induced on a net (or a set of nets) by a switching net (or set of switching nets). Nets with any circuit topology can be analyzed by this metric. The metric can be computed by inspection for most typical interconnects. It determines an upper bound on the coupled noise for RC and overdamped RLC interconnects. The paper is organized as follows. Section 2 presents the noise estimation technique, followed in Section 3 by techniques for efficient computation. Results are presented in Section 4 followed by conclusions.

2. Noise Estimation

Coupled noise in interconnect networks is caused by capacitive coupling between an active (or aggressor) net and a passive (or victim) net. Consider the circuit shown in Figure 1. For noise coupling, the aggressor net is the net that switches state, where as the victim net is quiet or maintains its present state. Figure 2 represents the general circuit model of the coupled noise problem, where the aggressor and victim nets can have any topologies. The victim net, the aggressor net and the coupling between them is represented by a linear circuit description.

1092-3152/97 $10.00 © 1997 IEEE

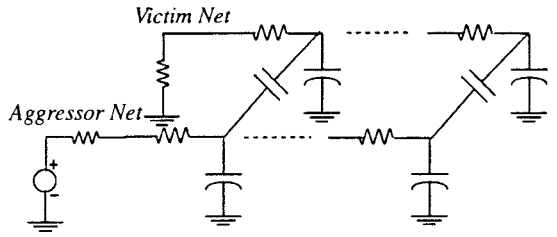

Figure 1 *Circuit schematic with aggressor and victim net for coupled noise.*

In general, the number of victim nets and number of aggressor nets may be more than one. Initially, the case with one victim and one aggressor is analyzed. This can be easily extended to the case with multiple victim and aggressor nets.

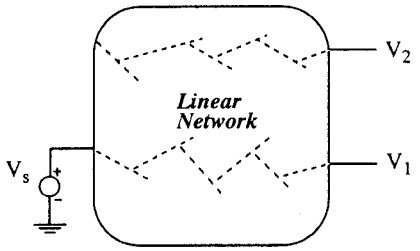

Figure 2 *General circuit representation for coupled noise.*

The circuit equations for circuit shown in Figure 2 can be written as

$$\begin{bmatrix} C_1 & C_c \\ C_c & C_2 \end{bmatrix} \begin{bmatrix} \dot{v}_1 \\ \dot{v}_2 \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} + \begin{bmatrix} B_1 \\ B_2 \end{bmatrix} v_s \tag{1}$$

where v_1 is a vector of node voltages in the aggressor net, v_2 is a vector of node voltages in the victim net, and v_s is the input to the aggressor net. Or, in the Laplace Domain,

$$sC_1V_1 + sC_cV_2 = A_{11}V_1 + A_{12}V_2 + B_1V_s \tag{2}$$

The first state equation in Equation (1) can be rewritten as,

$$V_1 = (sC_1 - A_{11})^{-1}[(A_{12} - sC_c)V_2 + B_1V_s] \tag{3}$$

For the coupled noise waveform V_2,

$$sC_cV_1 + sC_2V_2 = A_{21}V_1 + A_{22}V_2 + B_2V_s \tag{4}$$

Or, (5)

$$(sC_2 - A_{22})V_2 =$$

$$(A_{21} - sC_c)(sC_1 - A_{11})^{-1}[(A_{12} - sC_c)V_2 + B_1V_s] + B_2V_s \tag{6}$$

Alternatively,

$$[(sC_2 - A_{22}) - (A_{21} - sC_c)(sC_1 - A_{11})^{-1}(A_{12} - sC_c)]V_2 \tag{7}$$

$$= (A_{21} - sC_c)(sC_1 - A_{11})^{-1}B_1V_s + B_2V_s$$

However, the interconnect networks that cause coupled noise have special characteristics, which can be identified as follows.

[1]. $A_{12} = 0$

Non zero value of A_{12} would indicate a resistive or DC path from the aggressor net to victim net. It would mean that both the aggressor and victim net are electrically the same net or signal, which is not the case. Hence, A_{12} is zero for all coupled noise problems.

[2]. $A_{21} = 0$

Non zero value of A_{21} would indicate a resistive or DC path from the victim net to the aggressor net. It would mean that both the aggressor and victim net are electrically the same net or signal, which is not the case. Hence, A_{21} is zero for all coupled noise problems.

[3]. $B_2 = 0$

Non zero value of B_2 would indicate a resistive or DC path from the source, V_s, to the victim net as well as the aggressor net. It would mean that a source is directly exciting the victim net and notion of coupled noise is meaningless. Hence, B_2 is zero for all coupled noise problems.

Hence the circuit description of the coupled noise circuit, shown in Figure 2, can be rewritten as,

$$\begin{bmatrix} C_1 & C_c \\ C_c & C_2 \end{bmatrix} \begin{bmatrix} \dot{v}_1 \\ \dot{v}_2 \end{bmatrix} = \begin{bmatrix} A_{11} & 0 \\ 0 & A_{22} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} + \begin{bmatrix} B_1 \\ 0 \end{bmatrix} v_s \tag{8}$$

Hence Equation (6) can be simplified to,

$$[(sC_2 - A_{22}) - sC_c(sC_1 - A_{11})^{-1}sC_c]V_2 = -sC_c(sC_1 - A_{11})^{-1}B_1V_s \tag{9}$$

Let,

$$H(s) = \frac{V_2(s)}{V_s(s)} \tag{10}$$

As seen from Equation (9), $H(s)$ has a zero at $s = 0$. This is true for all networks that exhibit coupled noise. The zero at $s = 0$ is due to the fact that the coupling between the aggressor and victim net is purely capacitive.

The fact that $H(s)$ has a zero at $s = 0$ allows us to compute the maximum possible noise that can ever be induced on the victim net V_2. If the input to the circuit, V_s, is an infinite ramp, output of the aggressor net V_1 is also an infinite ramp, but it is delayed by the signal delay in the aggressor net. However, all nodes in the victim net exponentially chargeup to their respective finite maximum steady state value. If input to the circuit, V_s, is a finite ramp (which it typically is) or if the input is an infinite ramp, the derivative of coupled noise, $\dot{V}_2$, is zero at $t = \infty$ and the coupled noise V_2 has a finite maximum value.

The value of this finite maximum value can be computed from Equation (10) through use of the final value theorem.

Final value of $V_2(s)$ at $t = \infty$ is given by

$$V_{2,max} = \lim_{s \to 0} sV_2(s) \quad (11)$$

Or

$$V_{2,max} = \lim_{s \to 0} sH(s)u(s) = \lim_{s \to 0} sH(s)\frac{\dot{u}}{s^2} = \lim_{s \to 0} H(s)\frac{\dot{u}}{s} \quad (12)$$

Applying the final value theorem and combining it with Equation (9) yields,

$$V_{2,max} = -A_{22}^{-1}C_c A_{11}^{-1}B_1\dot{u} \quad (13)$$

Equation (13) gives the maximum amount of coupled noise that can be induced on the victim net V_2, for the given linear circuit, i.e. A_{11}, A_{22}, C_1, C_c and C_2, and the input slope, $\dot{u}$. Equation (13) yields an upper bound because the monotonicityy of the RC circuit response[7][8]. In the presence of the inductors, if the circuit is overdamped or critically damped, the monotonicity is still maintained.

3. Circuit Interpretation and Computation

The maximum coupled noise given by Equation (13) is relatively easy to evaluate. We will now present steps and necessary circuit conditions to further simplify the computation.

Equation (13) can be rewritten as,

$$V_{2,max} = A_{22}^{-1}C_c\dot{V}_{1,ss} \quad (14)$$

Where,

$$\dot{V}_{1,ss} = -A_{11}^{-1}B_1\dot{u} \quad (15)$$

Equation (14) can be rewritten as,

$$V_{2,max} = A_{22}^{-1}I_c \quad (16)$$

Where,

$$I_c = C_c\dot{V}_{1,ss}. \quad (17)$$

The computation of maximum coupled noise can be decomposed into the following three steps:

- Computation of $\dot{V}_{1,ss} = -A_{11}^{-1}B_1\dot{u}$. This requires circuit analysis of the Aggressor net.
- Computation of $I_c = C_c\dot{V}_{1,ss}$. This requires a multiplication step.
- Computation of $V_{2,max} = A_{22}^{-1}I_c$. This requires circuit analysis of the Victim net.

Step1: Computation of $\dot{V}_{1,ss}$

The computation of the steady state ramp derivative on the aggressor net is illustrated in Equation Figure 3. The input source is replaced by a voltage source of value equal to the input derivative, $\dot{V}_s$. All the capacitors in the aggressor net are replaced by open circuits and all coupling capacitors to the victim net are not considered in the this circuit. The solution of the circuit so obtained gives the steady state ramp derivative, $\dot{V}_{1,ss}$, at each corresponding node. The solution of this circuit involves the matrix factorization of the aggressor net's dissipative matrix. However, for typical interconnects, this solution is trivial as shown in the next subsection.

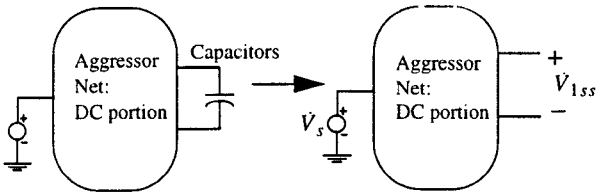

Figure 3 *Circuit Transformation to compute* $\dot{V}_{1,ss}$.

Step1: Typical Interconnects:

Figure 4 shows the computation of the steady state derivative for the aggressor net for typical interconnects. For on chip interconnects, the nets do not have a dissipative (or DC) path to ground. A dissipative path to ground in the interconnection would mean DC loss of signal, which typical is not the case for on chip interconnects.

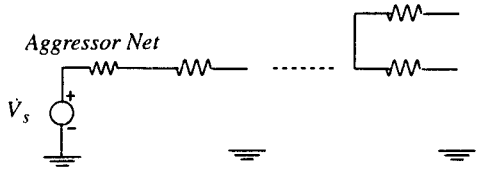

Figure 4 *Computation of* $\dot{V}_{1.ss}$ *for typical interconnects.*

In the typical case of no dissipative path to ground, computation of $\dot{V}_{1,ss}$ is trivial. In such a case, there is no current flow in the circuit shown in Figure 4, and $\dot{V}_{1,ss} = \dot{V}_s$.

In summary, $\dot{V}_{1,ss} = \dot{V}_s$, in case of no resistive path to ground in the aggressor net

Step2: Computation of I_c

This step involves a simple multiplication step that converts the steady state derivative of the aggressor net to a current on the victim net using the coupling capacitor matrix, C_c. For a node i in the victim net

$$I_i = \sum_{\forall j} C_{c,ij}\dot{V}_{1j,ss} \quad (18)$$

where $C_{c,ij}$ is the coupling capacitor between node i on the victim net(s) to node j on the aggressor net. $\forall j$ indicates the summation of all nodes in the aggressor net (or set of aggressor nets) capacitively coupled to node i on the victim net.

Step3: Computation of N_{max} or $V_{2,max}$

Figure 5 shows the computation of the maximum induced noise on the victim net. The capacitors on the victim net are replaced by the coupling currents, I_c, from the computation in step 2. Note that I_c is a vector of currents. Each capacitive node in the victim net is replaced by a current source of value corresponding to its index in the I_c vector. The voltage on a node in this circuit gives the maximum noise than can be coupled at that node. That is, the voltage of each node, say voltage $V_{2,i}$ at node i, gives the maximum noise that can be induced at the node i. The computation of the maximum induced noise requires a DC solution of the victim net. The cost of this DC solution is a single matrix factorization.

Step3: Typical Interconnects

Figure 6 shows the computation of the victim net for typical inter-

connects. As mentioned in the previous section, the solution of the maximum induced noise requires a DC solution of the victim net. This cost is in addition to the cost of DC solution of the aggressor net in order to determine the steady state derivative and coupling currents. However, as mentioned earlier, for typical interconnects, the solution of aggressor net is trivial and does not require any computation cost. Similarly, for typical interconnects, the solution of the victim net is also greatly simplified and requires only a linear time evaluation which can be carried out by inspection.

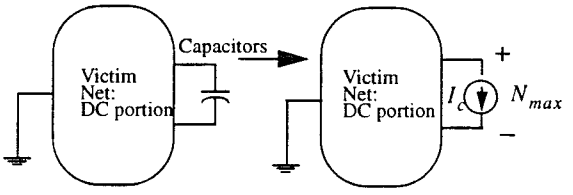

Figure 5 *Circuit transformation for computation of maximum noise* N_{max}.

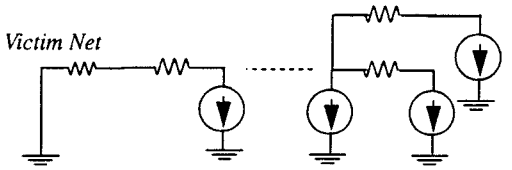

Figure 6 *Computation of* N_{max} *for typical interconnects.*

Consider the sample 3RC circuit in Figure 7 to illustrate the computation of N_{max} by inspection for typical interconnects.

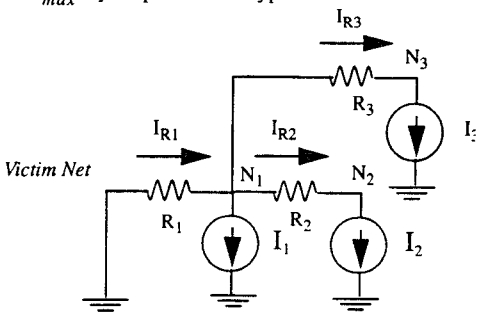

Figure 7 *Illustration of solution by inspection for maximum induced noise for typical interconnects.*

The maximum induced noise at each node can be written by inspection as,

$$N_{max,1} = V_{2.1} = -R_1(I_1 + I_2 + I_3) \tag{19}$$

$$N_{max,2} = V_{2.2} = -R_1(I_1 + I_2 + I_3) - R_2 I_2 \tag{20}$$

$$N_{max,3} = V_{2.3} = -R_1(I_1 + I_2 + I_3) - R_3 I_3 \tag{21}$$

The maximum coupled noise can also be written as,

$$N_{max,1} = -R_1(C_{c1} + C_{c2} + C_{c3})\dot{u} \tag{22}$$

$$N_{max,2} = -R_1(C_{c1} + C_{c2} + C_{c3})\dot{u} - R_2 C_{c2}\dot{u} \tag{23}$$

$$N_{max,3} = -R_1(C_{c1} + C_{c2} + C_{c3})\dot{u} - R_3 C_{c3}\dot{u} \tag{24}$$

In general, for a tree structure, the maximum induced noise, $N_{max,i}$, at node i can be computed as,

$$N_{max,i} = R_i \sum_{\forall L} I_j + N_{max,i-1} \tag{25}$$

Where $\forall L$ denotes the summation of all coupling currents at nodes which are in the load (i.e. in direction of the victim sink) of that particular node in the victim net. And $N_{max,i-1}$ denotes the noise at the previous node (towards the root of the tree).

Since the metric is an closed form expression, it can also be used to computed the maximum allowable coupling capacitance given the noise budget. This value of the coupling capacitance can then be used to compute the distance between the nets.

So the cost of computing the maximum coupled noise is the multiplication to computed the coupling currents and multiplications shown in Equation (25) to computed the coupled voltage. The complexity of this computation is significantly lower than either transient analysis through numerical integration or moment matching methods.

In the case of multiple aggressor nets, linear superposition is used. I_c in Equation (25) is computed for each aggressor net by multiplying its respective capacitive coupling by the respective input slope of each aggressor net. I_c 's from each aggressor net are added together to compute the total current which can then be used to compute the maximum noise. In case of timing orthogonality, the summation of currents from the aggressor nets has to be performed differently. Timing orthogonality, in this case, implies that the arrival time windows on the different aggressor nets are different. In such a case only the aggressor nets with overlapping arrival time windows have to be considered in computing the maximum noise on the victim net(s).

4. Results

The techniques described in the previous sections have been implemented in a noise computation tool. This section presents noise accuracy and computation speed results on various interconnect structures.

The peak coupled noise on the victim net for a typical small RC interconnect structure with a rise time of 200ps and power supply voltage of 1.8v is computed by circuit simulation and proposed metric. Table 1: summarizes the results for ten nodes in the circuit. As seen for the table, the proposed metric and the simulation results show an excellent match. Table 2: summarizes the peak coupled noise for the same circuit but with a faster rise time of 100ps and power supply of 1.8v. In this case, the metric is more conservative, over estimation the peak noise by 14.11% in the worst case. The accuracy of the metric degrades with reduction in rise times of the signal of the aggressor net. However, note that the peak noise predicted is always more than the actual obtained by simulation. If the rise time is small, like in the second example, the smaller rise time does not allow the circuit to reach the ramp steady state noise (which the metric predicts). Hence, the metric predicts a value of the peak noise which is greater than the actual peak noise.

The loading of the interconnect normally does not allow for very small rise times. The accuracy of the metric should normally be

acceptable for several noise verification, noise pruning and physical design applications.

Node	Circuit Simulation	Proposed Metric
1	0.0084	0.0084
2	0.0160	0.0160
3	0.0227	0.0227
4	0.0286	0.0286
5	0.0336	0.0336
6	0.0378	0.0379
7	0.0412	0.0412
8	0.0437	0.0438
9	0.0454	0.0454
10	0.0462	0.0463

Table 1: Comparison of Noise as computed by circuit simulation and the proposed metric. Units of noise are volts.

Node	Circuit Simulation	Proposed Metric	% Error
1	0.0147	0.0168	7.73%
2	0.0277	0.0319	13.1%
3	0.0392	0.0454	13.65%
4	0.0492	0.0572	13.98%
5	0.0578	0.0673	14.11%
6	0.0651	0.0757	14.00%
7	0.0709	0.0824	13.95%
8	0.0752	0.0875	14.05%
9	0.0782	0.0908	13.87%
10	0.0797	0.0925	13.83%

Table 2: Comparison of Noise as computed by circuit simulation and the proposed metric with rise time of 100ps. Units of noise are volts.

Table 3: shows the run time comparison of the proposed metric with an Krylov subspace based Arnoldi model reduction package for several RC circuits. These circuits are RC trees, with capacitive coupling between aggressor and victim net, and with no DC path to ground in the interconnect. The drivers are modeled by linear resistance and a voltage source, where as the victim net is modeled by a linear resistance. The computation of the metric is performed both through matrix factorization(Equation (13)) and by inspection(Equation (25)). The Arnoldi-based model reduction engine uses matrix solution to compute the circuit response. Hence, the comparison of the Arnold-based model reduction to the proposed metric (matrix factorization) is more appropriate. It should be noted that path tracing techniques can also be used in Arnoldi-based model reduction.

As seen from the table, for the matrix based comparison the metric shows significant computational advantage over the model reduction technique. The model reduction requires repeated matrix factorizations, solution for eigenvalues for the reduced system and time exponential evaluations. It should be noted however, that the model reduction technique can be used to obtain the complete transient response of the noise waveform. But, if only peak noise is of interest, which it is for several applications, the proposed metric is more efficient.

Circuit	Number of Elements	Arnoldi Model Reduction	Proposed Metric (Matrix Method)	Proposed Metric (By Inspection)
ckt1	500	.2s	.00s	.00s
ckt2	5,000	5.86s	.07s	.01s
ckt3	50,000	145s	3.44s	.05s
ckt4	500,000	-	360.55s	.35s

Table 3: Comparison of runtime for the proposed metric with model reduction techniques.

5. Conclusions

This paper has presented an efficient metric for computing the maximum coupled noise for on-chip interconnects. The noise metric can be used to compute noise in nets of any circuit topology. For typical interconnects, the noise can be computed in linear time. The computations can be performed by inspection instead of sparse matrix construction and factorization. The metric is an upper bound, with the error in estimation increasing with decrease in rise time. The techniques presented in this paper for noise computation are significantly more efficient than previous techniques, such as, moment matching methods or numerical integration.

6. References

[1]. R.R Tummala and E.J. Ryamszewski,"Microelectronics Packaging Handbook" Van Nostrand Reinhold, 1989.

[2]. K. Shephard and V. Narayan, *"Noise in Submicron Digital Design"*, IEEE/ACM International Conference on Computer Aided Design, Nov 1996.

[3]. L.W. Nagel. *SPICE2, A Computer Program to Simulate Semiconductor Circuits.* Technical Report ERL-M520, UC-Berkeley, May, 1975.

[4]. L. T. Pillage and R. A. Rohrer. Asymptotic Waveform Evaluation for Timing Analysis. *IEEE Trans. Computer-Aided Design.* 9(4):352-366, April, 1990.

[5]. P. Feldmann and R.W. Fruend, "Reduced-order modeling of large linear subcircuits via a block Lanczos algorithm", *In Proceedings of ACM/ IEEE Design Automation Conference*, pp. 474-479, 1995.

[6]. W.C.Elmore,"The Transient Response of Damped Linear Networks with particular regard to Broadband Amplifiers", *J. Applied Physics* 19,pp. 55-63, 1948.

[7]. P. Penfield and J. Rubinstein, "Signal delay in RC tree networks", *In Proceedings of ACM/IEEE Design Automation Conference*, pp. 613-617, 1981.

[8]. R. Gupta, B. Tutuianu and L.T.Pileggi, "The Elmore Delay as a Bound for RC Trees with Generalized Input Signals, *IEEE Transactions on Computer Aided Design*, Vol 16 No 1, pp. 95-104, Jan 1997.