Session 2: Analog Circuits

Lab
Power / Energy
Series / Parallel
Small Signal
Applications

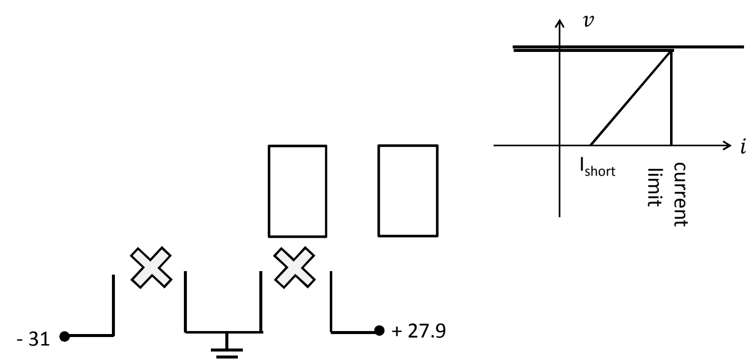
Outline

- Lab hits
  - Power Supply, Oscilloscope , Breadboard , Multimeters
- Energy
  - Power an Energy for R, L, C
- Series / Parallel
  - LTI & NLTI
  - Duality
  - 1-port 2-port Networks
  - Piecewise linear
- Small Signal
  - Bias point, small signal model
  - Diode example
- Applications
  - Rectifier, Voltage limiter
  - Zener

001

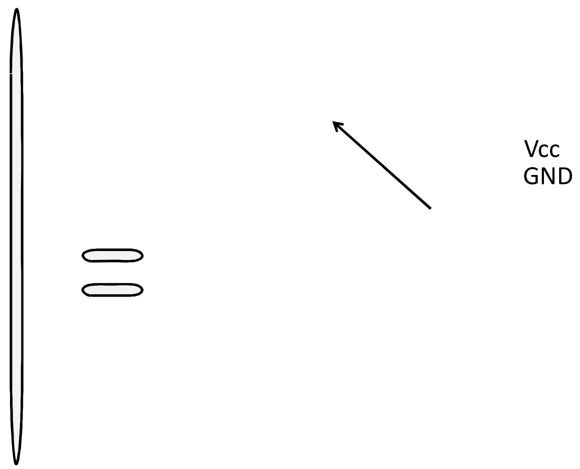
Lab

Power Supply



Breadboard

1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic



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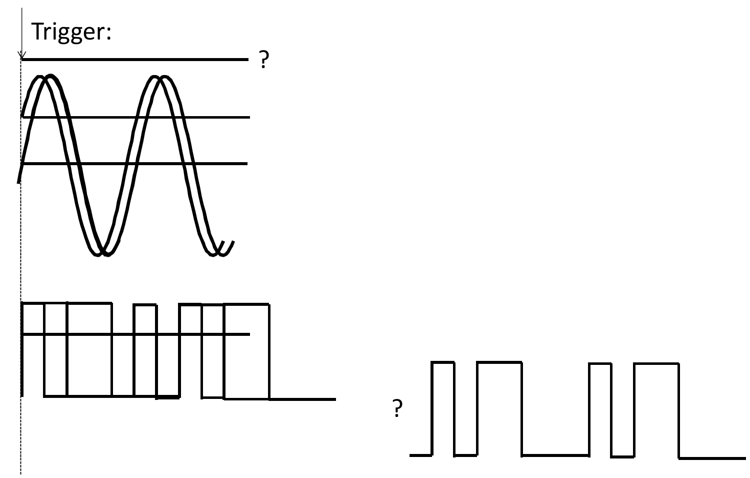
Oscilloscope

1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic



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Oscilloscope Probe

1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic

Do not use oscilloscope probe
for power cables!

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Digital Multimeters

1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic

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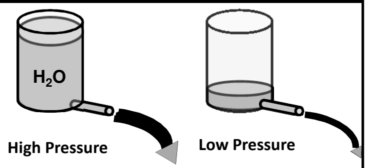
Energy and Power

1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic

Voltage definition: $V \equiv \frac{W}{Q}$

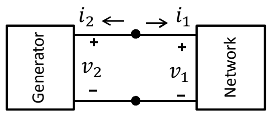
$$V = \frac{\delta W}{\delta Q} = \frac{\delta W/\delta t}{\delta Q/\delta t} = \frac{P}{I} \rightarrow P = VI$$



Power in electrical eng! $p(t) = v(t)i(t)$

$$W(t_0, t_1) \equiv \int_{t_0}^{t_1} p(t)dt = \int_{t_0}^{t_1} v(t)i(t)dt$$

$[J]$ ← W; $[W]$ ← $p(t)$



$$\begin{cases} v_1 = v_2 \\ i_1 = -i_2 \end{cases} \rightarrow p_1 = -p_2$$

$$\sum p = 0$$

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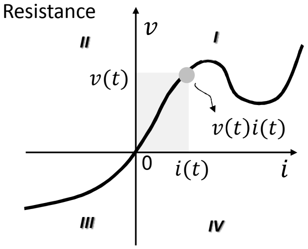
Passivity

1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic

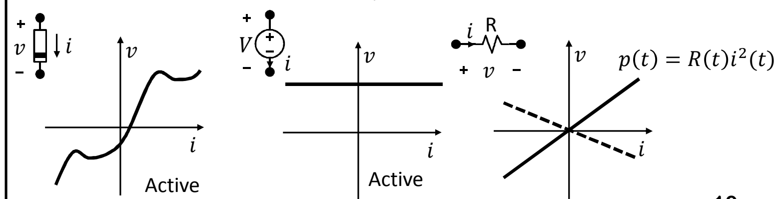
Resistance



Definition:

Passive
- always in I, II $\quad (\forall\, p(t) \geq 0)$
- receives power ; consumes power

Active: not passive
- a point in III or IV $\quad (\exists\, p(t) < 0)$
- delivers power ; generate power



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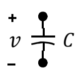
Energy stored in TI Capacitor

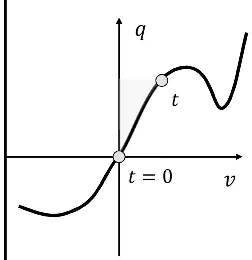
1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic

capacitance



NLTI $\quad q = \hat{q}\,(v) \qquad i(t) = \frac{dq}{dt}$

$$W(t_0, t_1) = \int_{t_0}^{t_1} v(t)\underbrace{i(t)\,dt}_{dq} = \int_{q(t_0)}^{q(t_1)} v(q)\,dq$$



Assume at $t = 0 : v = 0\,, q = 0$

$$\mathcal{E}_E(t) = \int_0^{q(t)} v(q)\,dq$$

If $q = Cv$

$$\mathcal{E}_E(t) = \tfrac{1}{2}Cv^2 = \frac{q^2}{2C}$$

Only for LTI Cap

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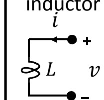
Energy stored in TI Inductor

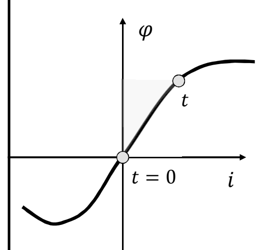
1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic

inductor



NLTI $\quad \varphi = \hat{\varphi}\,(i) \qquad v(t) = \frac{d\varphi}{dt}$

$$W(t_0, t_1) = \int_{t_0}^{t_1} i(t)\underbrace{v(t)\,dt}_{d\varphi} = \int_{\varphi(t_0)}^{\varphi(t_1)} i(\varphi)\,d\varphi$$



Assume at $t = 0 : i = 0\,, \varphi = 0$
(no hysteresis)

$$\mathcal{E}_M(t) = \int_0^{\varphi(t)} i(\varphi)\,d\varphi$$

If $\varphi = Li$

$$\mathcal{E}_M(t) = \tfrac{1}{2}Li^2 = \frac{\varphi^2}{2L}$$

Only for LTI Inductor

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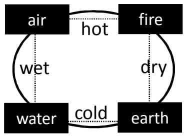
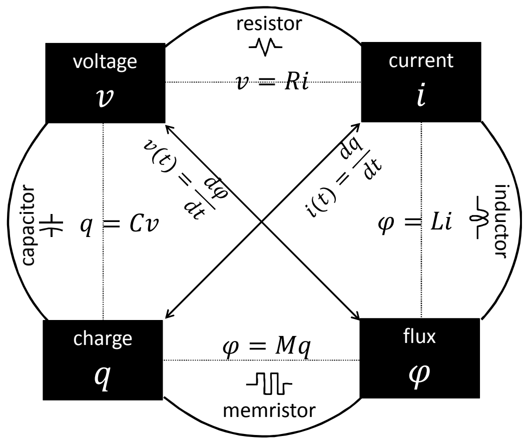
4th Element, Memristor

1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic





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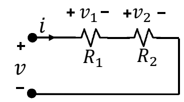
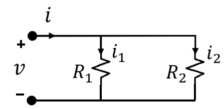
Series / Parallel LTI

1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic



$$i = i_1 = i_2$$
$$v = v_1 + v_2 \quad = (R_1+R_2)i$$
$$R_{eq} = (R_1+R_2)i$$



$$i = \frac{v}{R_{eq}} = i_1 + i_2 = \frac{v}{R_1} + \frac{v}{R_2}$$
$$G_{eq} = G_1 + G_2$$

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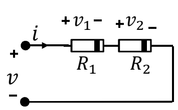
Series / Parallel NLTI

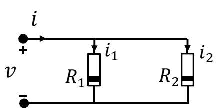
1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic



$$i = i_1 = i_2$$
$$v = \hat{R}_{eq}(i) = v_1 + v_2$$
$$= \hat{R}_1(i) + \hat{R}_2(i)$$

adding voltages at equal currents

true for current controlled



$$v = v_1 = v_2$$
$$i = \hat{G}_{eq}(v) = i_1 + i_2$$
$$= \hat{G}_1(v) + \hat{G}_2(v)$$

adding currents at equal voltages

true for voltage controlled

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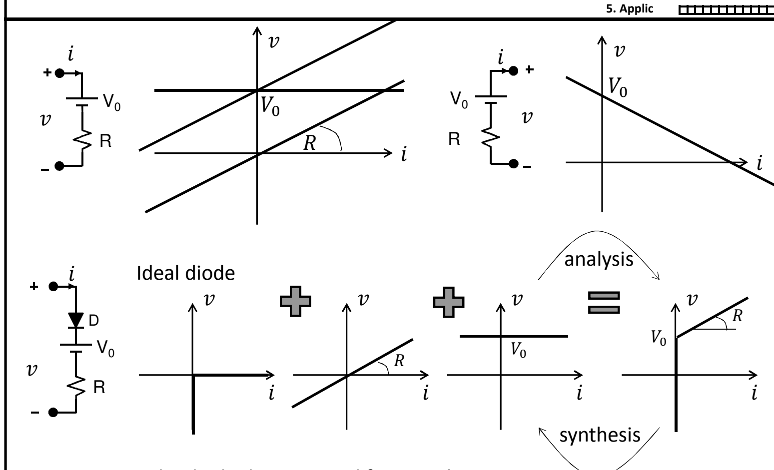
Series / Parallel NLTI

1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic



Reverse the diode direction and fine $v - i$ curve

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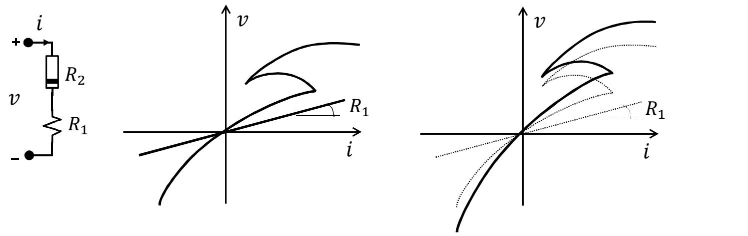
Series / Parallel NLTI



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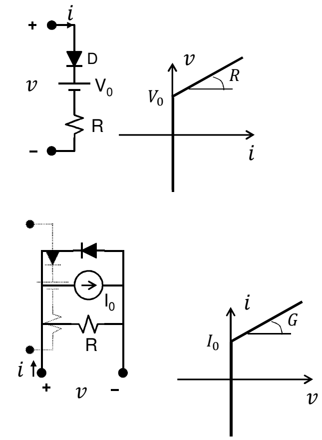
Duality

1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic



S	S*
v	i
$v = \hat{R}(i)$	$v = \hat{R}^{-1}(i) = G(v)$
R	$G = 1/R$
open circuit	short circuit
V_0	I_0
series	parallel
KVL	KCL

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?

1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic

- √ parallel /series combination of linear resistors will be linear
- × parallel /series combination of nonlinear resistors will be nonlinear
- √ parallel /series combination of bilateral resistors will be bilateral
- √ parallel /series combination of voltage controlled resistors will be voltage controlled

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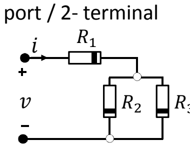
2-port equal resistance

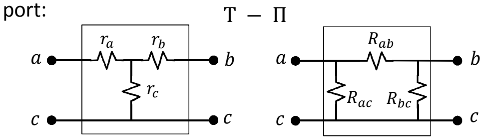
1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic

1- port / 2- terminal



2- port:

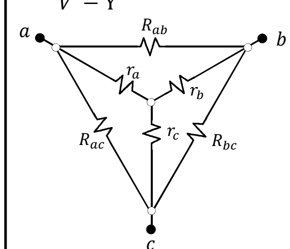
$\mathrm{T} - \Pi$



3 eqs , 3 unknown

$$\begin{cases} r_a + r_c = R_{ac} \parallel (R_{ab} + R_{bc}) \\ r_b + r_c = R_{bc} \parallel (R_{ab} + R_{ac}) \\ r_a + r_b = R_{ab} \parallel (R_{ac} + R_{bc}) \end{cases}$$

$\nabla - \mathrm{Y}$



$$r_a = \frac{R_{ac}\,R_{ab}}{R_{ac} + R_{ab} + R_{bc}}$$

$$r_b = \frac{R_{bc}\,R_{ab}}{R_{ac} + R_{ab} + R_{bc}}$$

$$r_a = \frac{R_{ac}\,R_{bc}}{R_{ac} + R_{ab} + R_{bc}}$$

$$R_{ab} = \frac{r_a r_b + r_a r_c + r_b r_c}{r_c}$$

$$R_{bc} = \frac{r_a r_b + r_a r_c + r_b r_c}{r_a}$$

$$R_{ac} = \frac{r_a r_b + r_a r_c + r_b r_c}{r_b}$$

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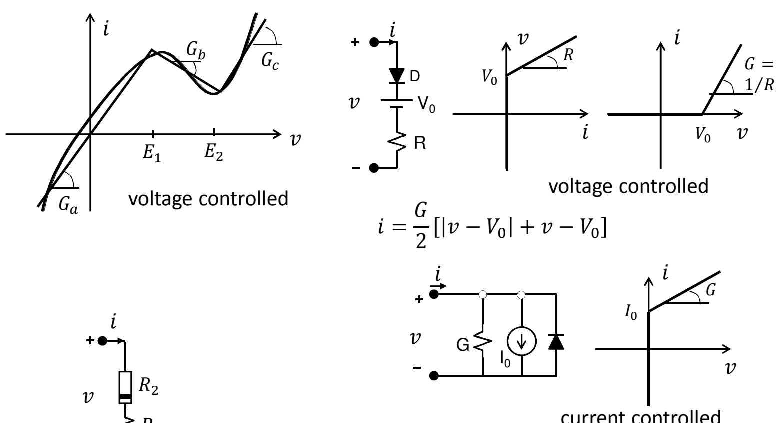
Piecewise Linear Approximation Technique – Synthesis

1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic



$$i = \frac{G}{2}\left[|v - V_0| + v - V_0\right]$$

$$v = \frac{R}{2}\left[|i - I_0| + i - I_0\right]$$

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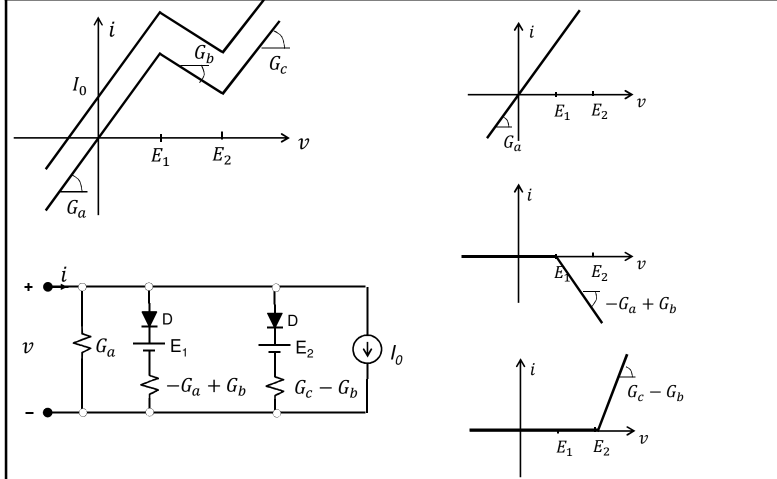
Piecewise Linear Approximation Technique – Synthesis

1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic



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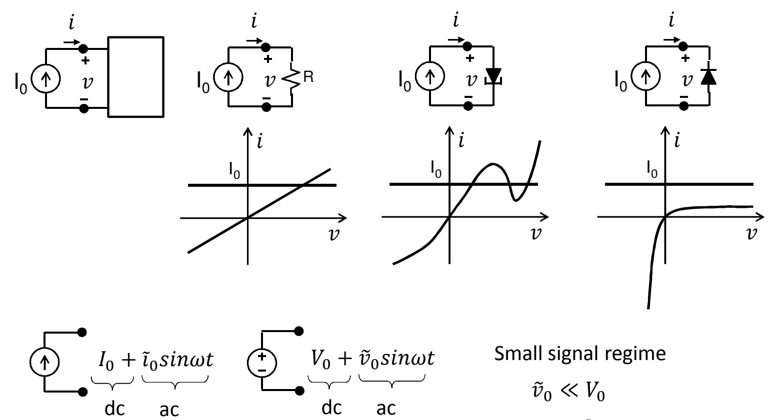
Quiescent Point

1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic



$I_0 + \tilde{i}_0 sin\omega t$

$V_0 + \tilde{v}_0 sin\omega t$

Small signal regime

$\tilde{v}_0 \ll V_0$

$\tilde{i}_0 \ll I_0$

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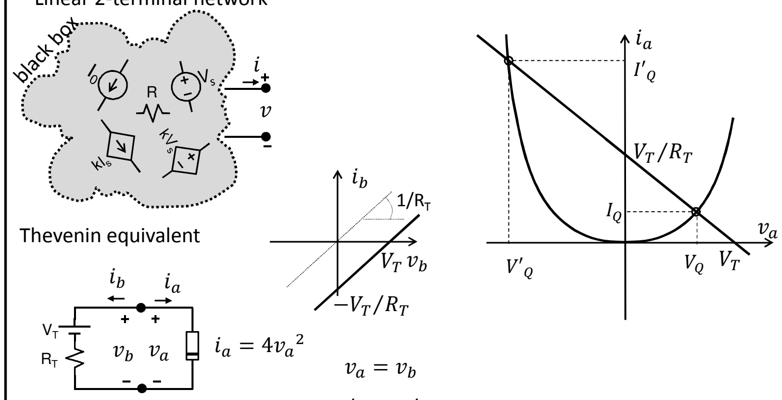
Quiescent (Bias) Point for NLTI

1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic

Linear 2-terminal network



Thevenin equivalent

$i_a = 4{v_a}^2$

$v_a = v_b$

$i_a = -i_b$

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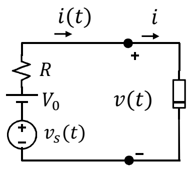
Small-Signal Analysis (for NLTI)

1. Lab 2. Power 3. Ser/Parl 4. Small sig. 5. Applic



$v_s(t) = \tilde{v}_0 sin\omega t$

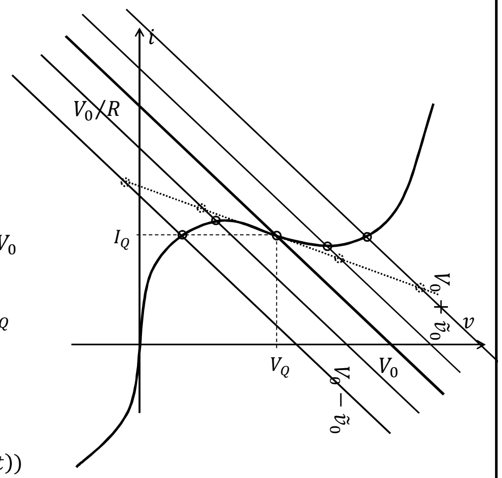
Small-signal condition $\tilde{v}_0 \ll V_0$

$i = \hat{\imath}(v)$ $\begin{cases} I_Q = \hat{\imath}(V_Q) \\ V_Q = V_0 - RI_Q \end{cases}$

$v(t) \equiv V_Q + \tilde{v}(t)$

$i(t) \equiv I_Q + \tilde{\imath}(t)$

$I_Q + \tilde{\imath}(t) = \hat{\imath}(V_Q + \tilde{v}(t))$



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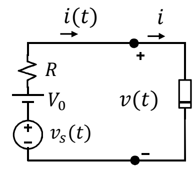
Small-Signal Analysis (for NLTI)

1. Lab 2. Power 3. Ser/Parl 4. Small sig. 5. Applic



$v_s(t) = \tilde{v}_0 sin\omega t$

Small-signal condition $\tilde{v}_0 \ll V_0$

$i = \hat{\imath}(v)$ $\begin{cases} I_Q = \hat{\imath}(V_Q) \\ V_Q = V_0 - RI_Q \end{cases}$

$v(t) \equiv V_Q + \tilde{v}(t)$

$i(t) \equiv I_Q + \tilde{\imath}(t)$

$I_Q + \tilde{\imath}(t) = \hat{\imath}(V_Q + \tilde{v}(t))$

Taylor series:

$$f(x_0 + \delta x) \cong f(x_0) + \left.\frac{df}{dx}\right|_{x_0} (\delta x) + \tfrac{1}{2}\left.\frac{d^2 f}{dx^2}\right|_{x_0} (\delta x^2) + \cdots$$

$$I_Q + \tilde{\imath}(t) \approx \hat{\imath}(V_Q) + \left.\frac{d\hat{\imath}}{dv}\right|_{V_Q} \tilde{v}(t)$$

dc $I_Q = \hat{\imath}(V_Q)$

ac $\tilde{\imath}(t) \approx \underbrace{\left.\frac{d\hat{\imath}}{dv}\right|_{V_Q}}_{G_{SS} = 1/R_{SS}} \tilde{v}(t)$

R_{SS} small signal resistance

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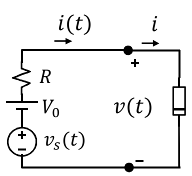
Small-Signal Analysis (for NLTI)

1. Lab 2. Power 3. Ser/Parl 4. Small sig. 5. Applic



Small-signal condition

$\tilde{v}_0 \ll V_0$

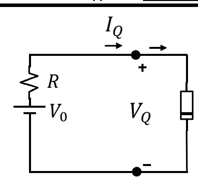
$v(t) \equiv V_Q + \tilde{v}(t)$

$i(t) \equiv I_Q + \tilde{\imath}(t)$

$\tilde{\imath}(t) \approx \frac{1}{R_{SS}} \tilde{v}(t)$

$R_{SS} = \frac{1}{\left.\frac{d\hat{\imath}}{dv}\right|_{V_Q}} = \left.\frac{dy}{dx}\right|_{I_Q}$

Step1:
Find Bias Point!

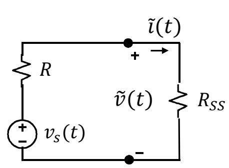


$R_{SS} = \frac{1}{\left.\frac{d\hat{\imath}}{dv}\right|_{V_Q}} = \left.\frac{dy}{dx}\right|_{I_Q}$

Step2:
Small Signal Analysis!

$\tilde{v}(t) = \frac{R_{SS}}{R + R_{SS}} v_s(t)$

$v_s(t) = \tilde{v}_0 sin\omega t$



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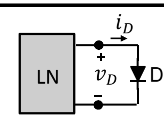
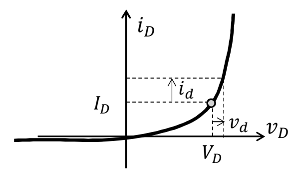
Example – Diode

1. Lab 2. Power 3. Ser/Parl 4. Small sig. 5. Applic





$\begin{cases} v_D = V_D + v_d \\ i_D = I_D + i_d \end{cases}$

bias small signal

NLTI: Diode

$$i_D = I_s\left(e^{qv_D/nkT} - 1\right)$$

$$V_T = \left.\frac{kT}{q}\right|_{300°K} = 26mV$$

Forward biased diode: $i_D = I_s\left(e^{qv_D/nkT} - 1\right) \approx I_s e^{\frac{V_D}{nV_T}} e^{\frac{v_d}{nV_T}}$

$$i_D \approx I_s e^{\frac{V_D}{nV_T}} \left(1 + \frac{v_d}{nV_T} + \tfrac{1}{2}\left(\frac{v_d}{nV_T}\right)^2 + \cdots\right) \approx I_D + \underbrace{I_D \frac{v_d}{nV_T}}_{i_d}$$

$\frac{v_d}{nV_T} \ll 1$

$r_d \equiv \frac{v_d}{r_d} = \frac{nV_T}{I_D}$ small signal resistance $r_d = \frac{1}{\left.\frac{di}{dv}\right|_{V_D}} = \frac{nV_T}{I_D}$

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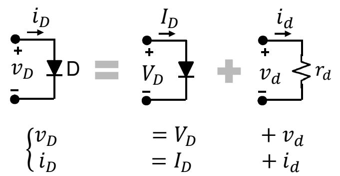
Example – Diode

1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic

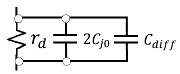


$$\begin{cases} v_D = V_D + v_d \\ i_D = I_D + i_d \end{cases}$$

bias   small signal

small signal resistance

$$r_d = \frac{nV_T}{I_D}$$



? How to solve bias (large signal) $I_D = I_s\left(e^{V_D/nV_T} - 1\right)$

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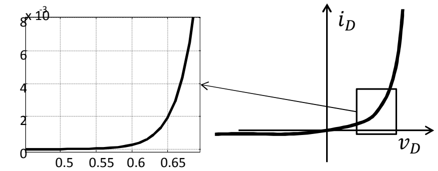
Diode – Large Signal

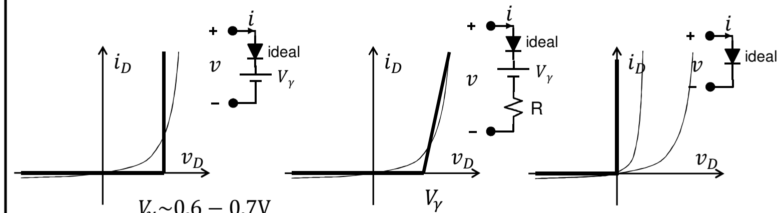
1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic



NLTI: Diode

$$i_D = I_s\left(e^{qv_D/nkT} - 1\right)$$

$$V_T = \left.\frac{kT}{q}\right|_{300°K} = 26mV$$



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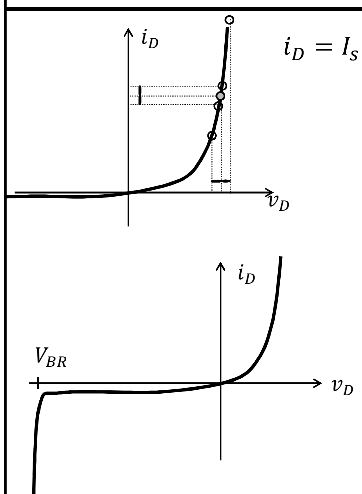
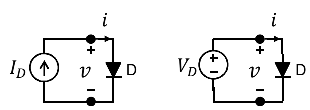
Diode – Large Signal

1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic



$$i_D = I_s\left(e^{qv_D/nkT} - 1\right)$$

? How we should bias a diode?



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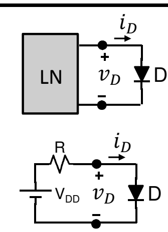
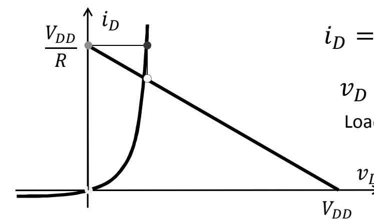
Example – Diode – Large Signal

1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic





$$i_D = I_s\left(e^{qv_D/nkT} - 1\right)$$

$$v_D = V_{DD} - i_D R$$

Load line

$V_{DD} = 5V$, $R = 1k\Omega$, $I_S = 5 \times 10^{-14}A$, $V_T = 26mV$

iteration

$v_D = 0 \rightarrow i_D = \frac{V_{DD} - v_D}{R} = 5mA$

$v_D = V_T \ln\left(\frac{i_D}{I_S}\right) = 0.658 \rightarrow i_D = \frac{V_{DD} - v_D}{R} = 4.341mA$

$v_D = V_T \ln\left(\frac{i_D}{I_S}\right) = 0.654864 \rightarrow i_D = \frac{V_{DD} - v_D}{R} = 4.345mA$

$v_D = V_T \ln\left(\frac{i_D}{I_S}\right) = 0.654889 \rightarrow i_D = \cdots$

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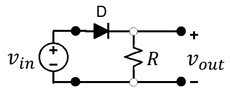
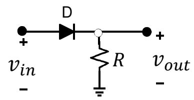
Example – Diode – Large/Small Signal

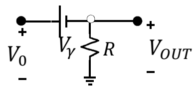
1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic



$v_{in} = V_0 + \hat{v}_i sin\omega t$



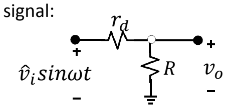
Bias:



$V_{OUT} = V_0 - V_\gamma$ $\quad I_D = \frac{V_0 - V_\gamma}{R}$

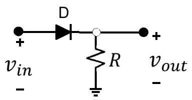
$r_d = \frac{nV_T}{I_D}$ small signal resistance

Small signal:



$v_o = \frac{R}{R + r_d} \hat{v}_i sin\omega t$

$v_{in} =$
$V_0 + \hat{v}_i sin\omega t$



$v_{out} = (V_0 - V_\gamma) + \frac{R}{R + r_d} \hat{v}_i sin\omega t$

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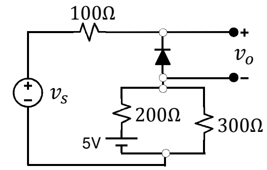
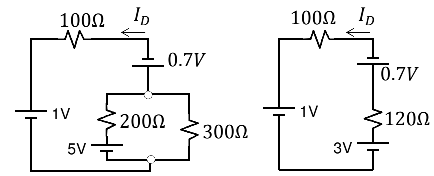
Example – Diode – Large/Small Signal

1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic

$v_s = 1V + 0.1V sin\omega t \; ; V_\gamma = 0.7V$



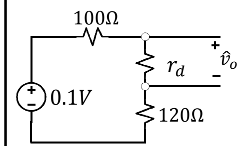
DC / bias



$I_D = \frac{3 - 1 - 0.7}{100 + 120} = 6.36mA$

$r_d = \frac{V_T}{I_D} = 3.9\Omega$

AC / small signal



$\hat{v}_o = \frac{r_d}{220 + r_d} 0.1 = 1.75mV$

$v_o = -0.7 + 1.75mV sin\omega t$

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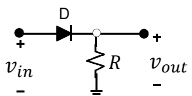
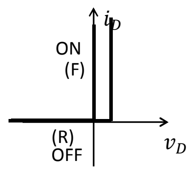
Example 01

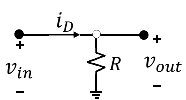
1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic



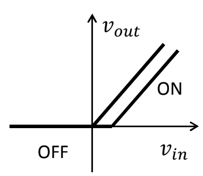
Find $v_{in} - v_{out}$ assume $V_\gamma = 0, 0.7V$



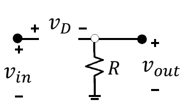
1: (F)
If $i_D > 0$



$v_{out} = v_{in}$
condition $i_D > 0$
$\rightarrow i_D = v_{out}/R > 0 \rightarrow v_{out} > 0$
$v_{in} > 0$



1: (R)
If $v_D < 0$



v_{out} =0 condition $v_D < 0$
$\rightarrow v_{in} - v_{out} < 0 \rightarrow v_{in} < 0$

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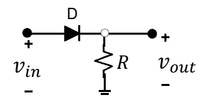
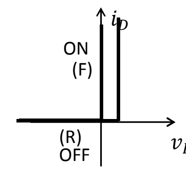
Example 01

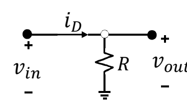
1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic



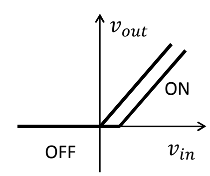
Find $v_{in} - v_{out}$ assume $V_\gamma = 0, 0.7V$



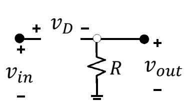
1: (F)
If $i_D > 0$



$v_{out} = v_{in}$
condition $i_D > 0$
$\rightarrow i_D = v_{out}/R > 0 \rightarrow v_{out} > 0$
$v_{in} > 0$



1: (R)
If $v_D < 0$



v_{out} =0 condition $v_D < 0$
$\rightarrow v_{in} - v_{out} < 0 \rightarrow v_{in} < 0$

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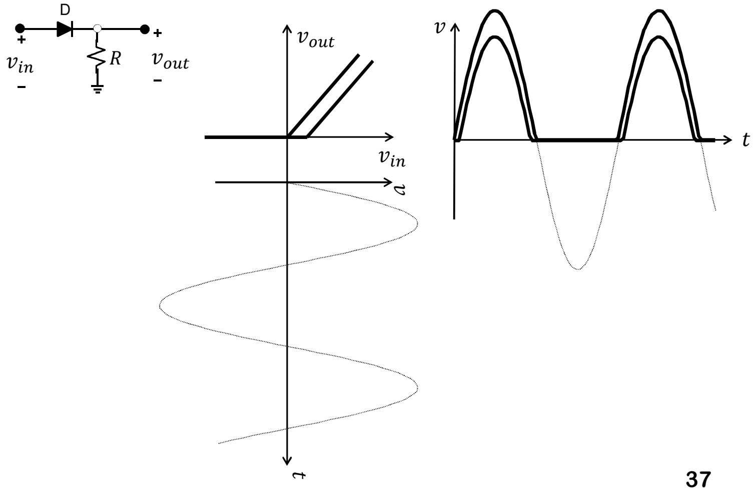
Example 01



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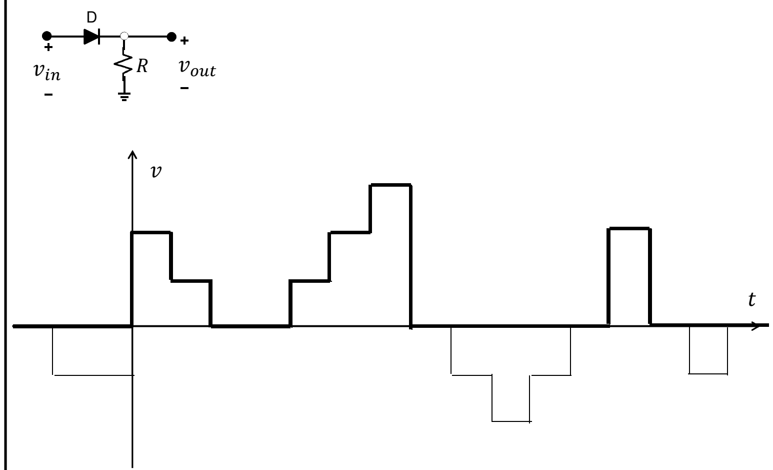
Example 01

1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic



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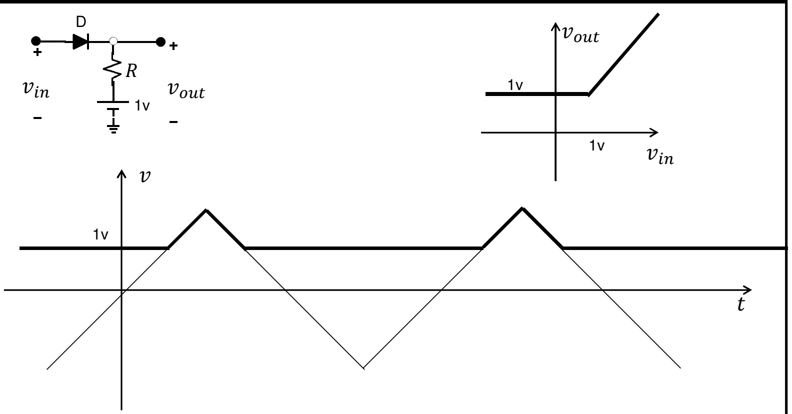
Example 01

1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic



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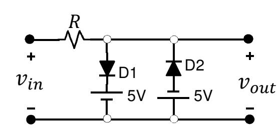
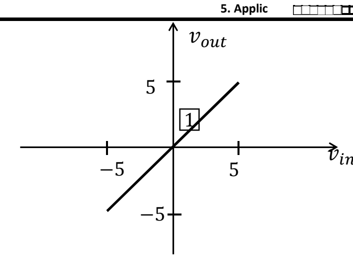
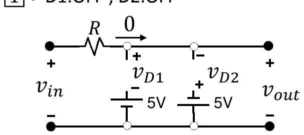
Voltage Limiter

1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic





1 : D1:OFF , D2:OFF



$v_{out} = v_{in}$

$v_{D1} < 0 \rightarrow v_{out} - 5 < 0 \rightarrow v_{out} < 5$

$v_{D2} < 0 \rightarrow -v_{out} - 5 < 0 \rightarrow v_{out} > -5$

condition $v_D < 0$
$\rightarrow v_{in} - v_{out} < 0 \rightarrow v_{in} < 0$

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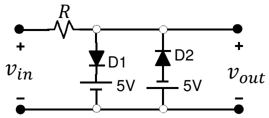
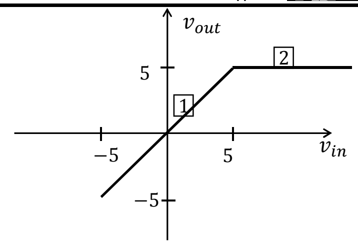
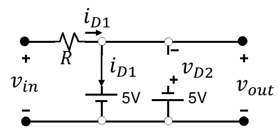
Voltage Limiter





2 : D1:ON , D2:OFF

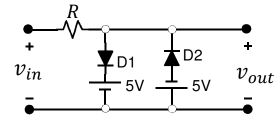


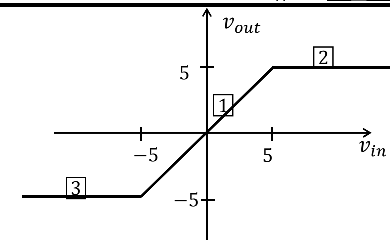
$v_{out} = 5V$

$v_{D2} = -5 - v_{out} = -10 < 0$ √

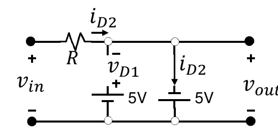
$i_{D1} = \frac{v_{in} - 5}{R} > 0 \rightarrow v_{in} > 5$

Voltage Limiter





3 : D1:OFF , D2:ON

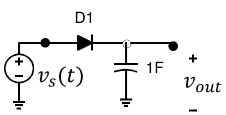


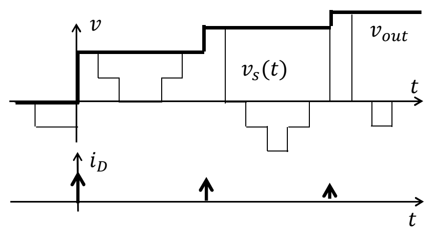
$v_{out} = -5V$

$v_{D1} = v_{out} - 5 = -10 < 0$ √

$i_{D2} = \frac{-v_{in} - 5}{R} > 0 \rightarrow v_{in} < -5$

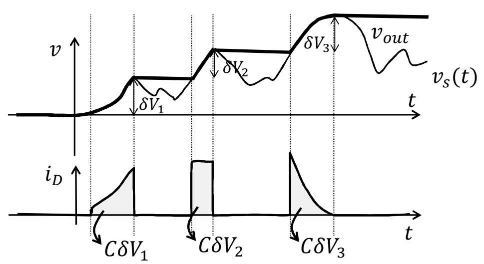
Peak Detector



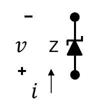


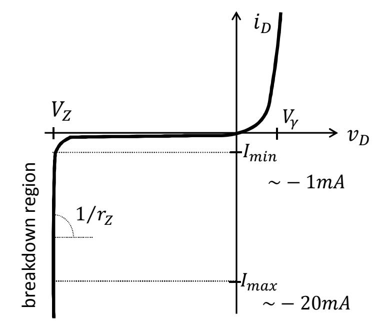
$i_D = i_C = C\frac{dv_{out}}{dt}$

$Q = CV$



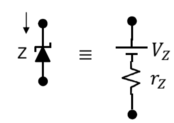
Zener Diode





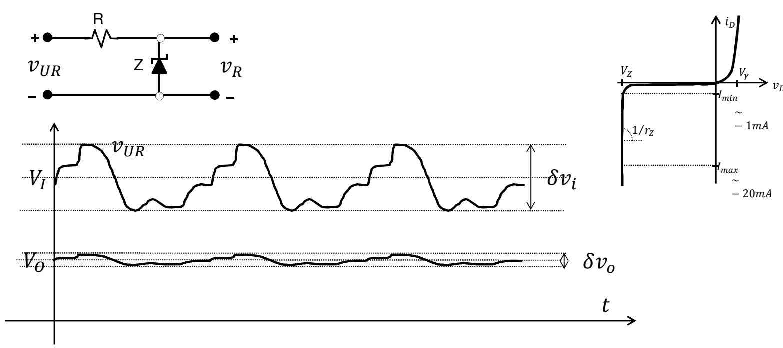
$P_{max} = I_{max}V_Z$

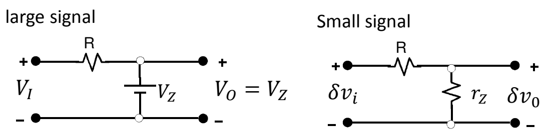
In breakdown region:



Zener Diode – Voltage Regulator

1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic





$$\delta v_0 = \frac{r_Z}{r_Z + R}\delta v_i$$

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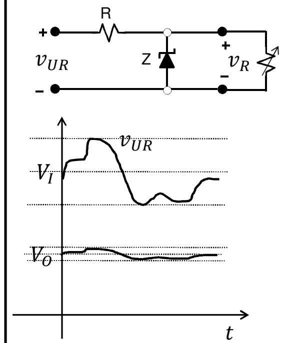
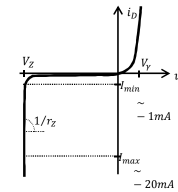
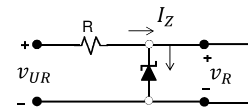
Zener Diode – Voltage Regulator

1. Lab
2. Power
3. Ser/Parl
4. Small sig.
5. Applic

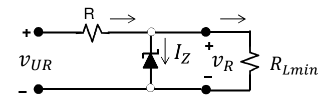


$R_{Lmin} < R_L < \infty$





$I_Z < I_{max}$ $\quad \frac{v_{URmax} - V_Z}{R} < I_{max}$



$I_Z > I_{min}$ $\quad \frac{v_{URmin} - V_Z}{R} - \frac{V_Z}{R_{Lmin}} > I_{min}$

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